

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR2450W85*	8500	$T_{vj} = -40^{\circ} \text{C to } 125^{\circ} \text{C}$, $I_{DRM} = I_{RRM} = 300\text{mA}$, $V_{DRM}, V_{RRM} t_p = 10\text{ms}$, $V_{DSM} \text{ \& } V_{RSM} =$ $V_{DRM} \text{ \& } V_{RRM} + 100\text{V}$ respectively
DCR2450W80	8000	
DCR2450W75	7500	
DCR2450W70	7000	

Lower voltage grades available.
 * 8200V @ -40°C , 6500V @ 0°C

KEY PARAMETERS

V_{DRM}	8500V
$I_{T(AV)}$	2450A
I_{TSM}	35200A
dV/dt^*	1500V/μs
dI/dt	300A/μs

* Higher dV/dt selections available

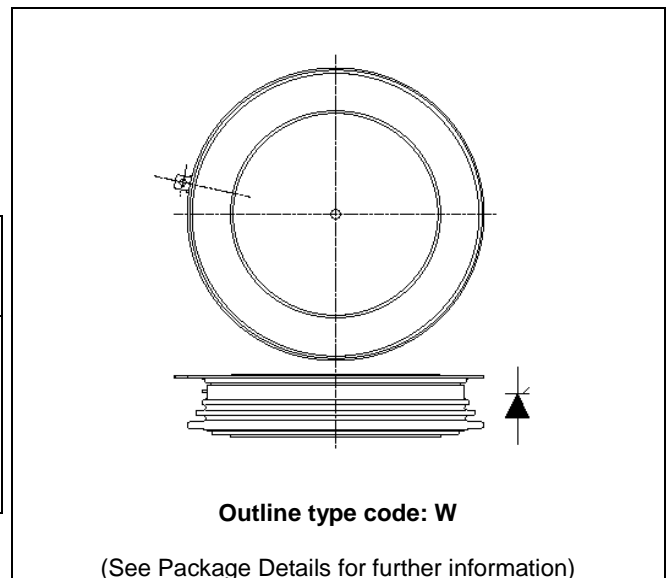


Fig. 1 Package outline

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR2450W85

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

CURRENT RATINGS

$T_{case} = 60^{\circ} C$ unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	2445	A
$I_{T(RMS)}$	RMS value	-	3840	A
I_T	Continuous (direct) on-state current	-	3750	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ} C$	35.2	kA
I^2t	I^2t for fusing	$V_R = 0$	6.2	MA ² s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.00631	$^{\circ} C/W$
		Single side cooled	Anode DC	-	0.01115	$^{\circ} C/W$
			Cathode DC	-	0.01453	$^{\circ} C/W$
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 76.0kN (with mounting compound)	Double side	-	0.0014	$^{\circ} C/W$
			Single side	-	0.0028	$^{\circ} C/W$
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}	-	125	$^{\circ} C$	
T_{stg}	Storage temperature range		-55	125	$^{\circ} C$	
F_m	Clamping force		68.0	84.0	kN	

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM} , $T_{case} = 125^{\circ}C$	-	300	mA	
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM} , $T_j = 125^{\circ}C$, gate open	-	1500	V/ μs	
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to $2x I_{T(AV)}$	Repetitive 50Hz	-	150	A/ μs
		Gate source 30V, 10 Ω , $t_r < 0.5\mu s$, $T_j = 125^{\circ}C$	Non-repetitive	-	300	A/ μs
$V_{T(TO)}$	Threshold voltage – Low level	500 to 2400A at $T_{case} = 125^{\circ}C$	-	1.037	V	
	Threshold voltage – High level	2400 to 7200A at $T_{case} = 125^{\circ}C$	-	1.229	V	
r_T	On-state slope resistance – Low level	500A to 2400A at $T_{case} = 125^{\circ}C$	-	0.487	m Ω	
	On-state slope resistance – High level	2400A to 7200A at $T_{case} = 125^{\circ}C$	-	0.398	m Ω	
t_{gd}	Delay time	$V_D = 67\% V_{DRM}$, gate source 30V, 10 Ω $t_r = 0.5\mu s$, $T_j = 25^{\circ}C$	-	3	μs	
t_q	Turn-off time	$T_j = 125^{\circ}C$, $V_R = 200V$, $dI/dt = 1A/\mu s$, $dV_{DR}/dt = 20V/\mu s$ linear	-	1000	μs	
Q_S	Stored charge	$I_T = 2000A$, $T_j = 125^{\circ}C$, $dI/dt = 1A/\mu s$,	2800	9000	μC	
I_L	Latching current	$T_j = 25^{\circ}C$, $V_D = 5V$	-	3	A	
I_H	Holding current	$T_j = 25^{\circ}C$, $R_{G-K} = \infty$, $I_{TM} = 500A$, $I_T = 5A$	-	300	mA	

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V _{GT}	Gate trigger voltage	V _{DRM} = 5V, T _{case} = 25° C	1.5	V
V _{GD}	Gate non-trigger voltage	At 50% V _{DRM} , T _{case} = 125°C	0.4	V
I _{GT}	Gate trigger current	V _{DRM} = 5V, T _{case} = 25° C	400	mA
I _{GD}	Gate non-trigger current	At 50% V _{DRM} , T _{case} = 125°C	10	mA

CURVES

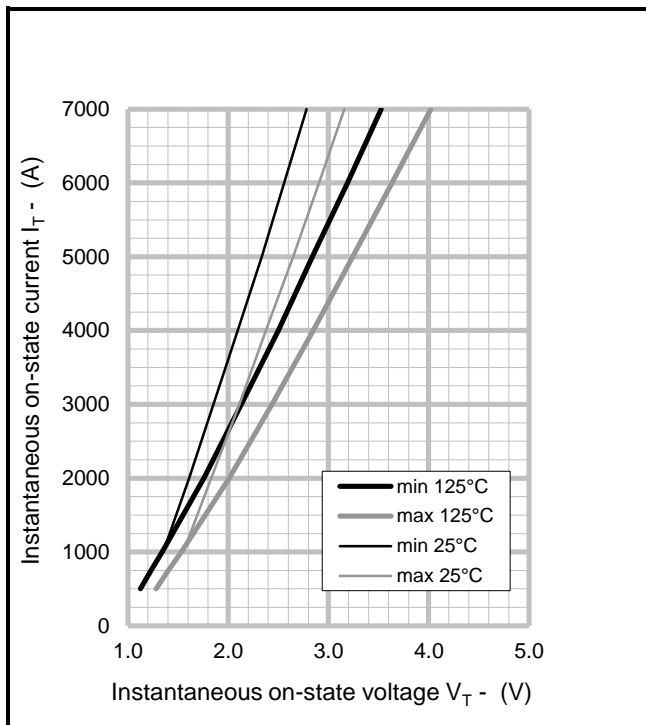


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

where A = 0.907134

B = -0.011004

C = 0.000304

D = 0.012936

these values are valid for T_j = 125°C for I_T 500A to 7200A

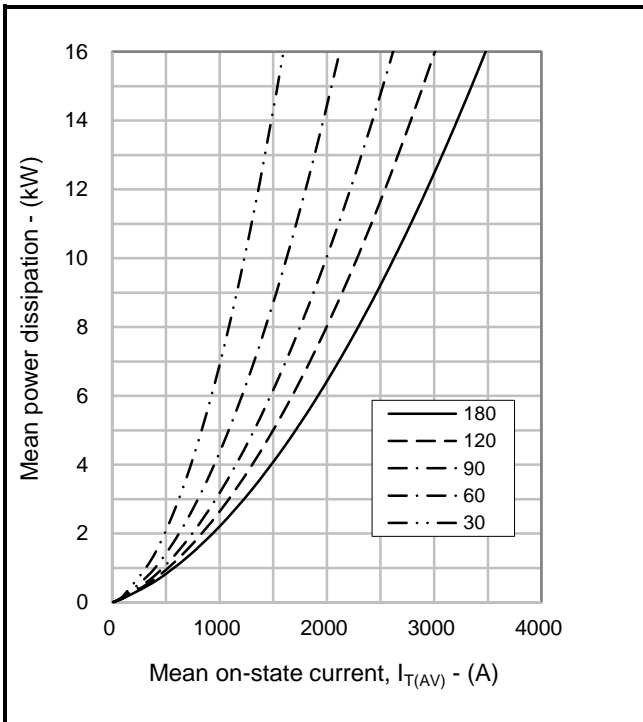


Fig.3 On-state power dissipation – sine wave

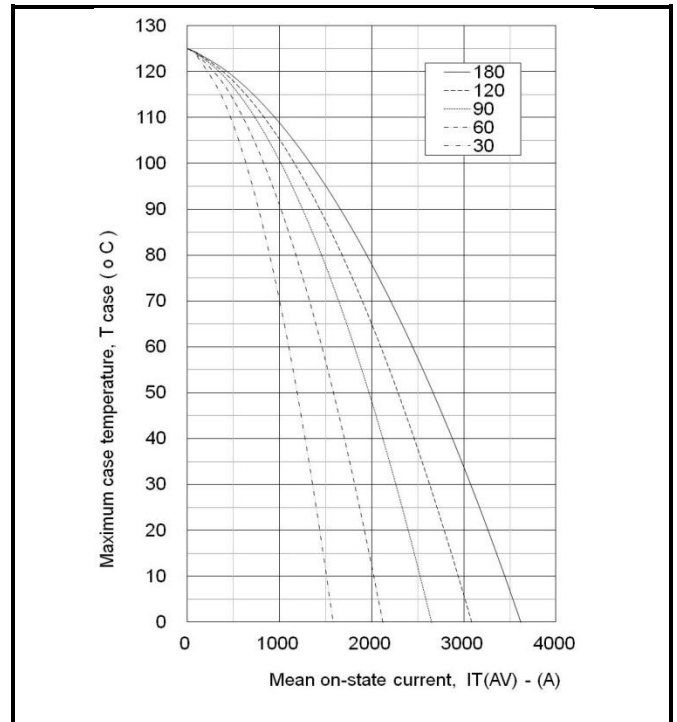


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

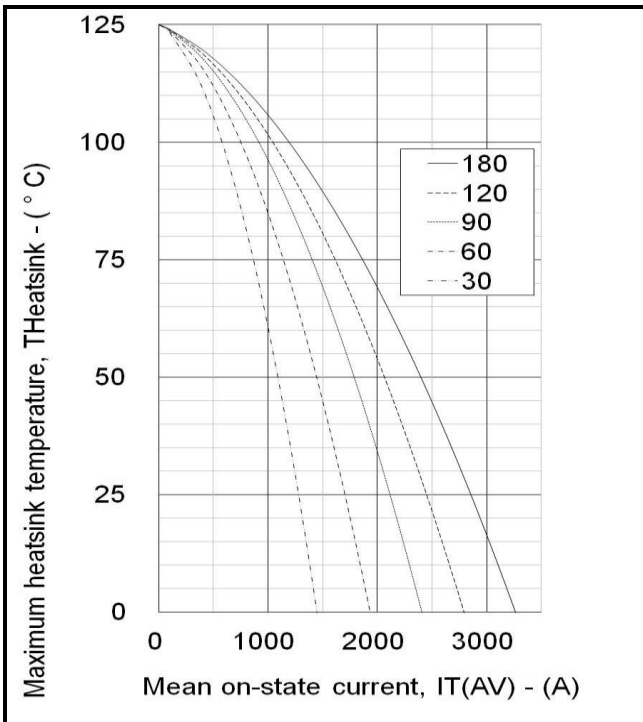


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

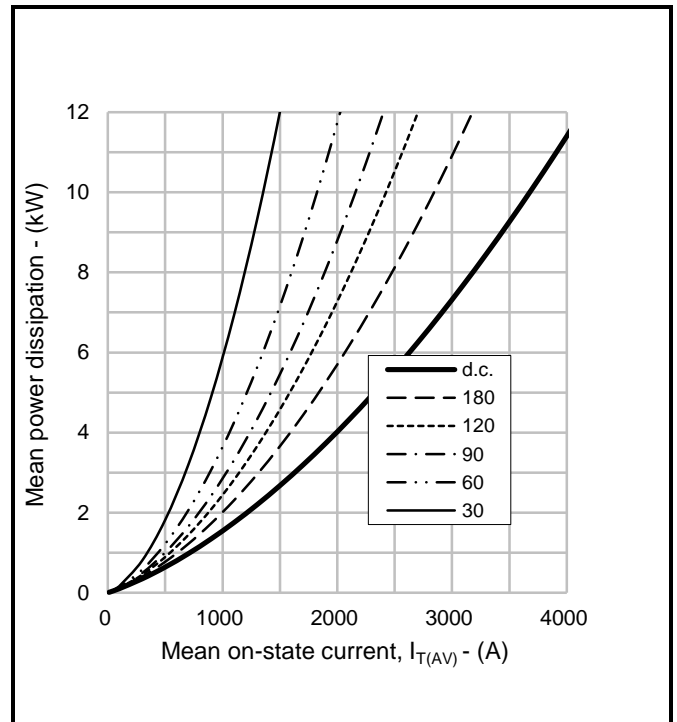


Fig.6 On-state power dissipation – rectangular wave

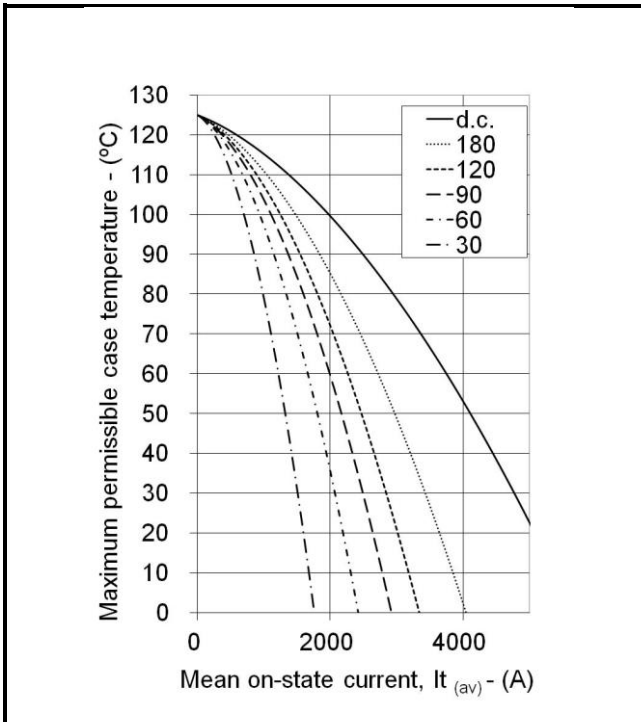


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

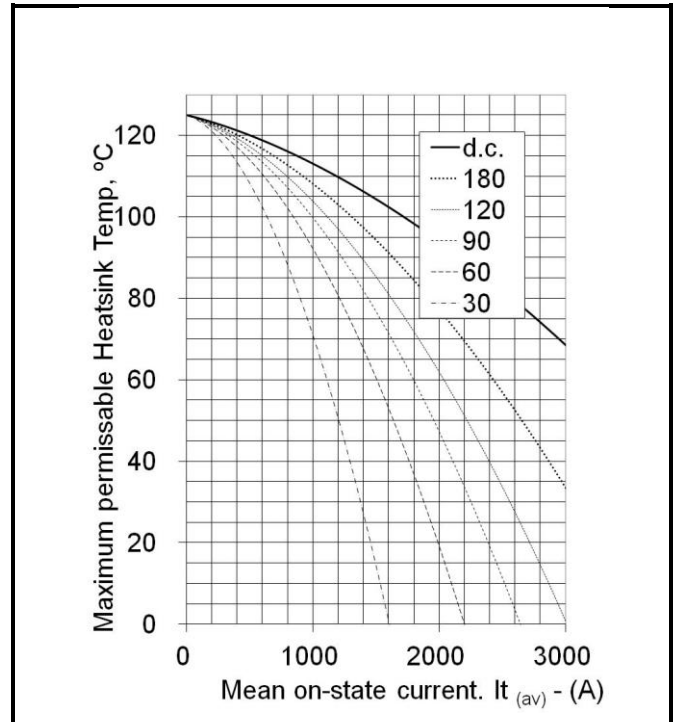


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave

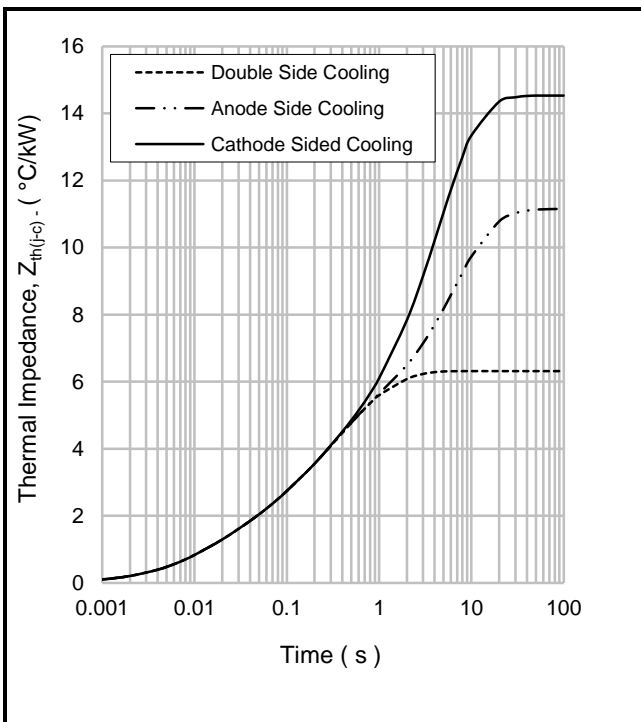


Fig.9 Maximum (limit) transient thermal impedance – junction to case (° C/kW)

		1	2	3	4
Double side cooled	R_i (°C/kW)	0.8816	1.2993	2.8048	1.3305
	T_i (s)	0.0106818	0.058404	0.3584979	1.1285
Anode side cooled	R_i (°C/kW)	1.5197	3.2398	5.7622	0.6312
	T_i (s)	0.0170581	0.2424644	6.013	15.364
Cathode side cooled	R_i (°C/kW)	1.4106	2.4667	6.7451	3.9054
	T_i (s)	0.0158344	0.1786951	3.6201	6.196

$$Z_{th} = \sum [R_i \times (1 - \exp. (-t/t_i))] \quad [1]$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

θ°	Double side cooling	
	sine.	rect.
180	1.00	0.67
120	1.16	0.97
90	1.33	1.13
60	1.48	1.31
30	1.61	1.51
15	1.66	1.61

θ°	Anode Side Cooling	
	sine.	rect.
180	0.94	0.64
120	1.08	0.91
90	1.23	1.06
60	1.37	1.22
30	1.47	1.38
15	1.52	1.47

θ°	Cathode Sided Cooling	
	sine.	rect.
180	0.95	0.65
120	1.09	0.92
90	1.25	1.07
60	1.38	1.23
30	1.49	1.40
15	1.54	1.49

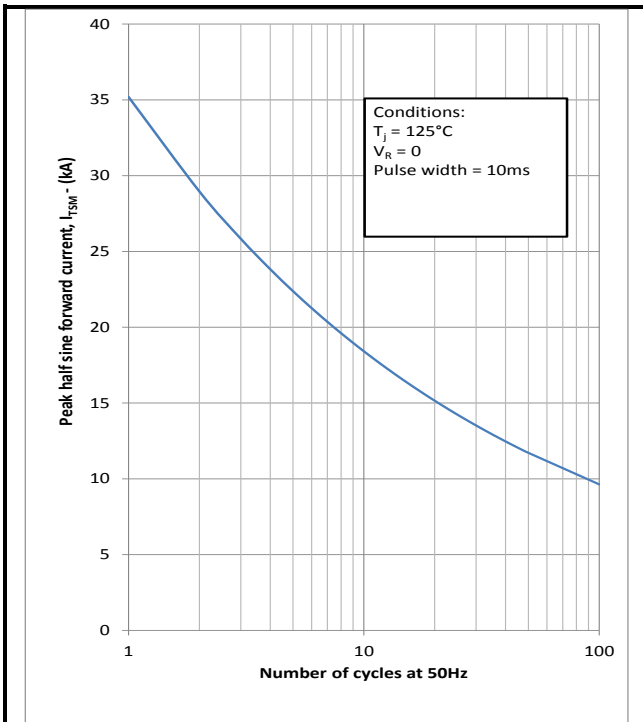


Fig.10 Multi-cycle surge current

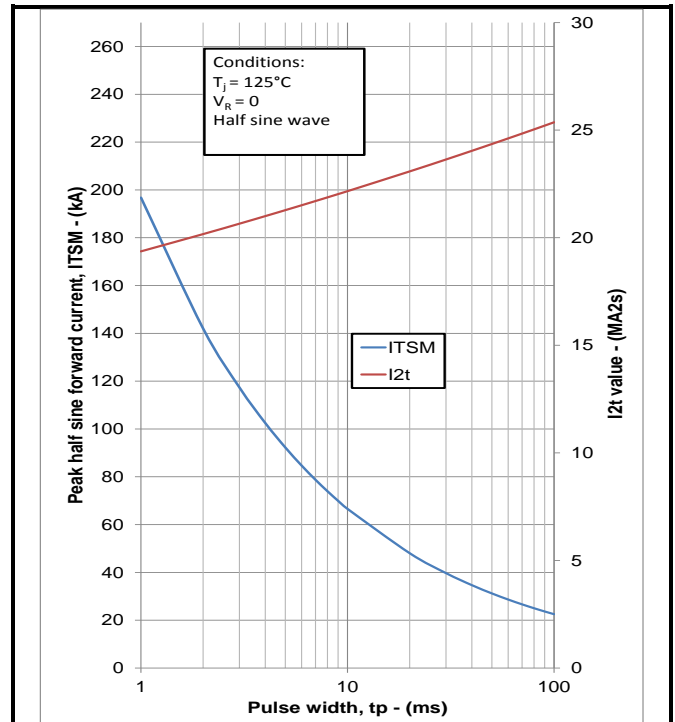


Fig.11 Single-cycle surge current

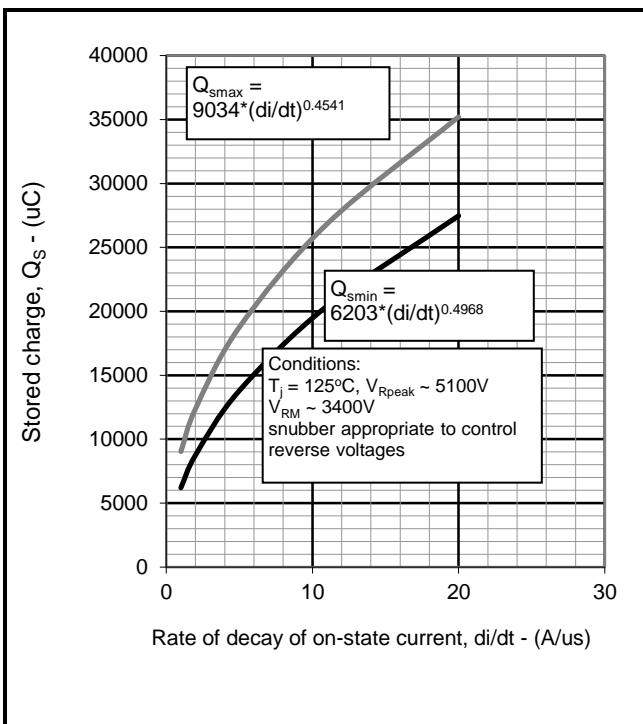


Fig.10 Reverse recovery charge

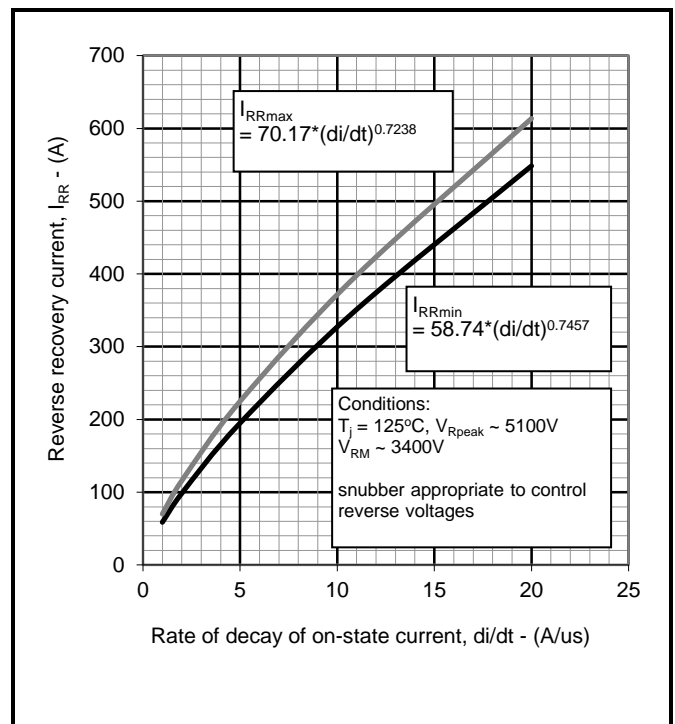


Fig.11 Reverse recovery current

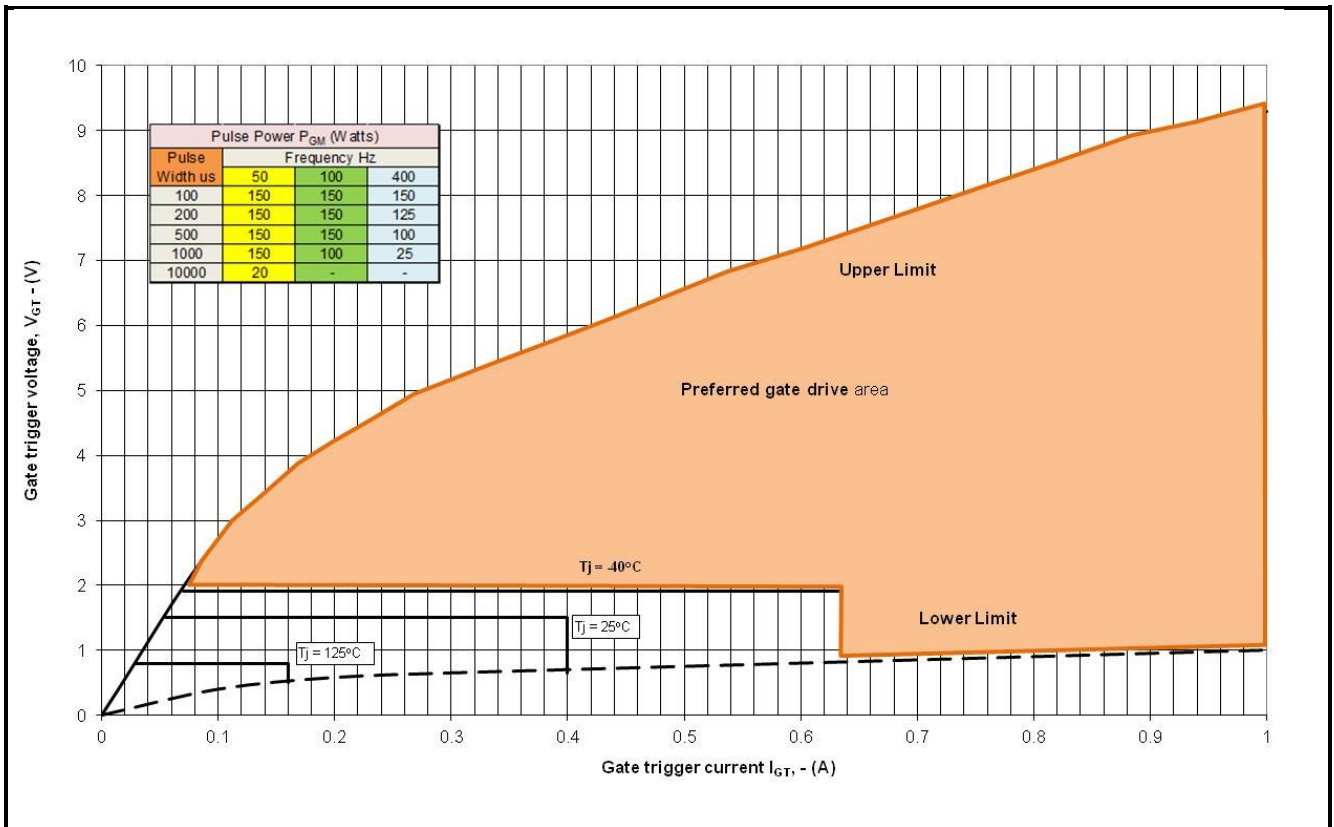


Fig12 Gate Characteristics

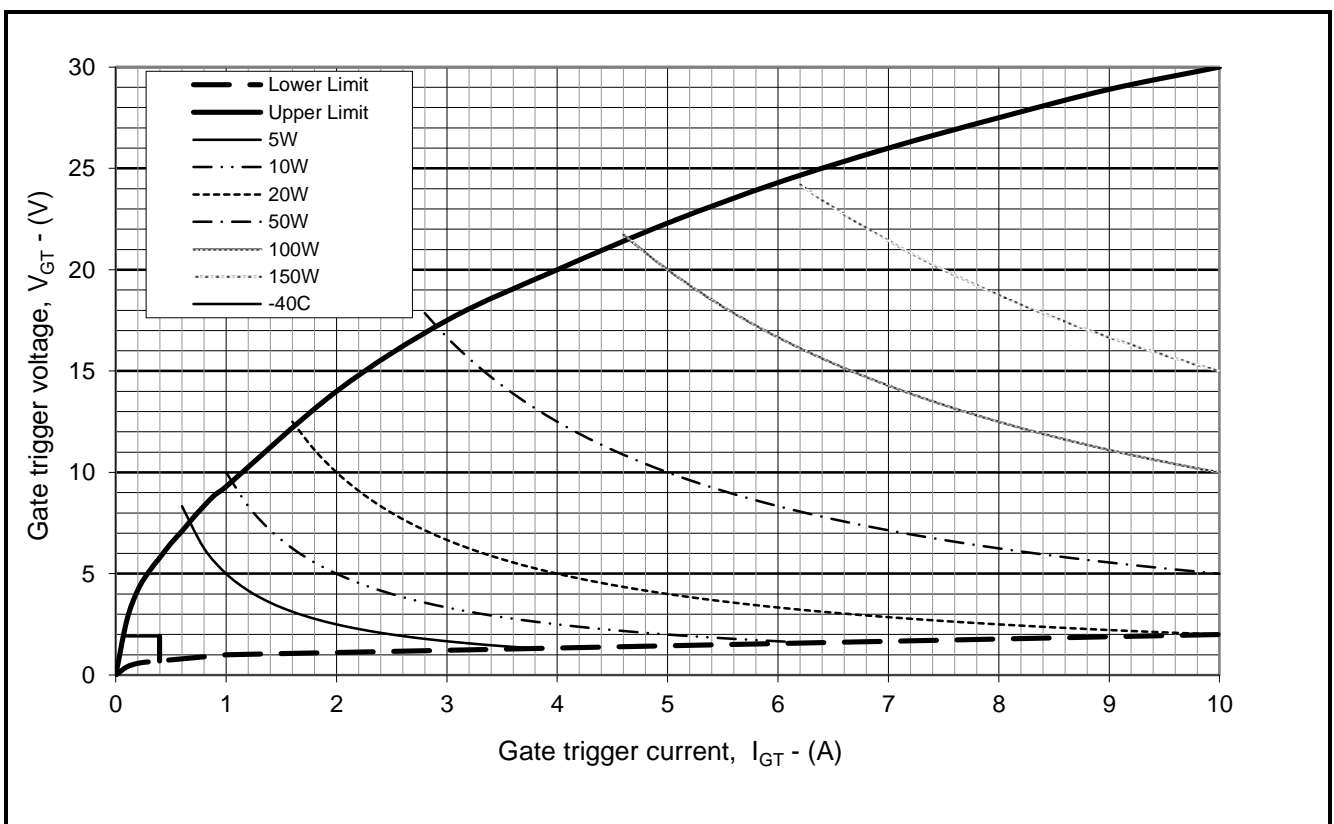


Fig. 13 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. **DO NOT SCALE.**

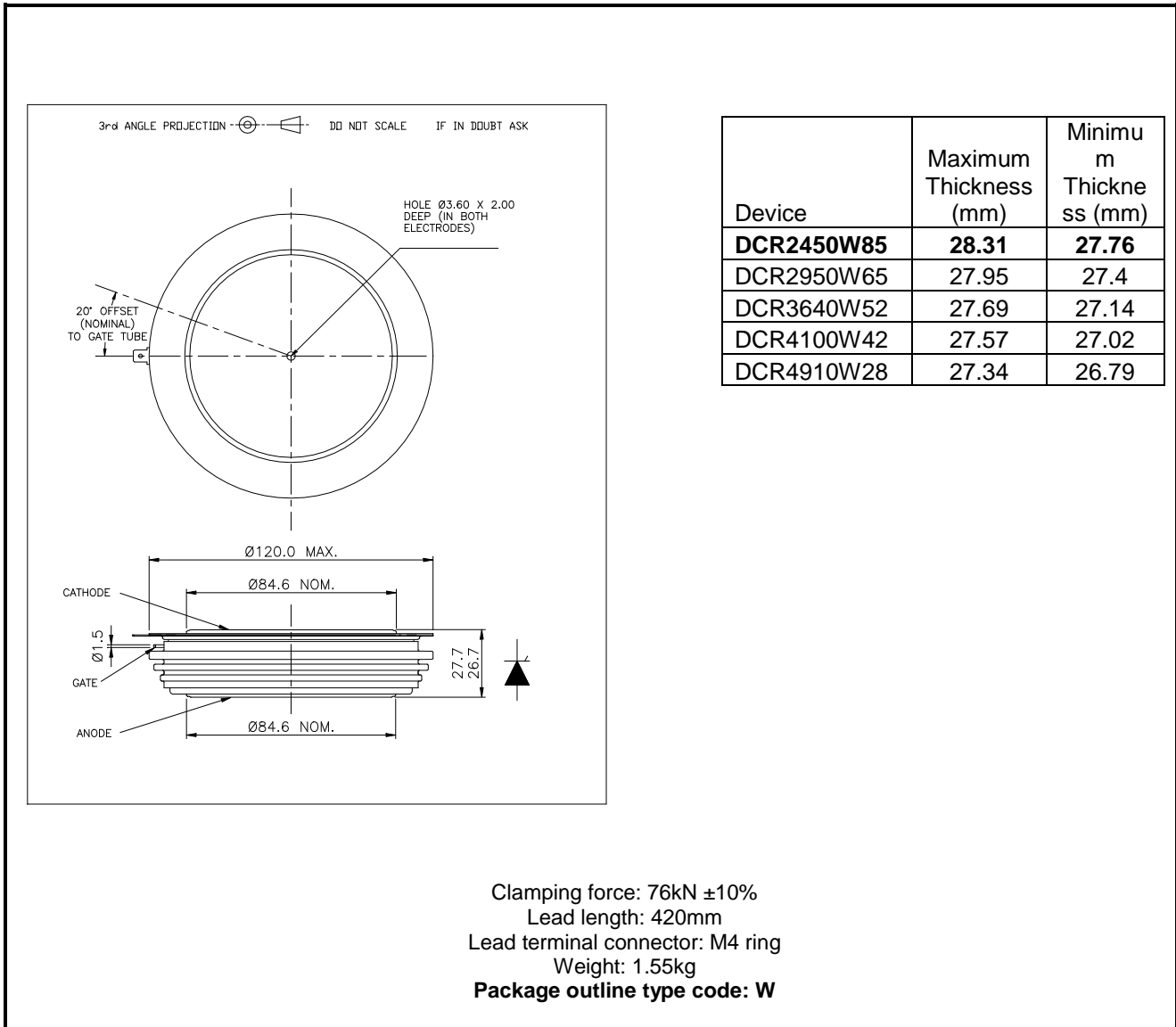


Fig.14 Package outline

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