REAL-TIME CLOCK WITH SERIAL I²C INTERFACE IDT1339

General Description

The IDT1339 serial real-time clock (RTC) is a low-power clock/date device with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially through an I²C bus. The clock/date provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The IDT1339 has a built-in power-sense circuit that detects power failures and automatically switches to the backup supply, maintaining time, date, and alarm operation.

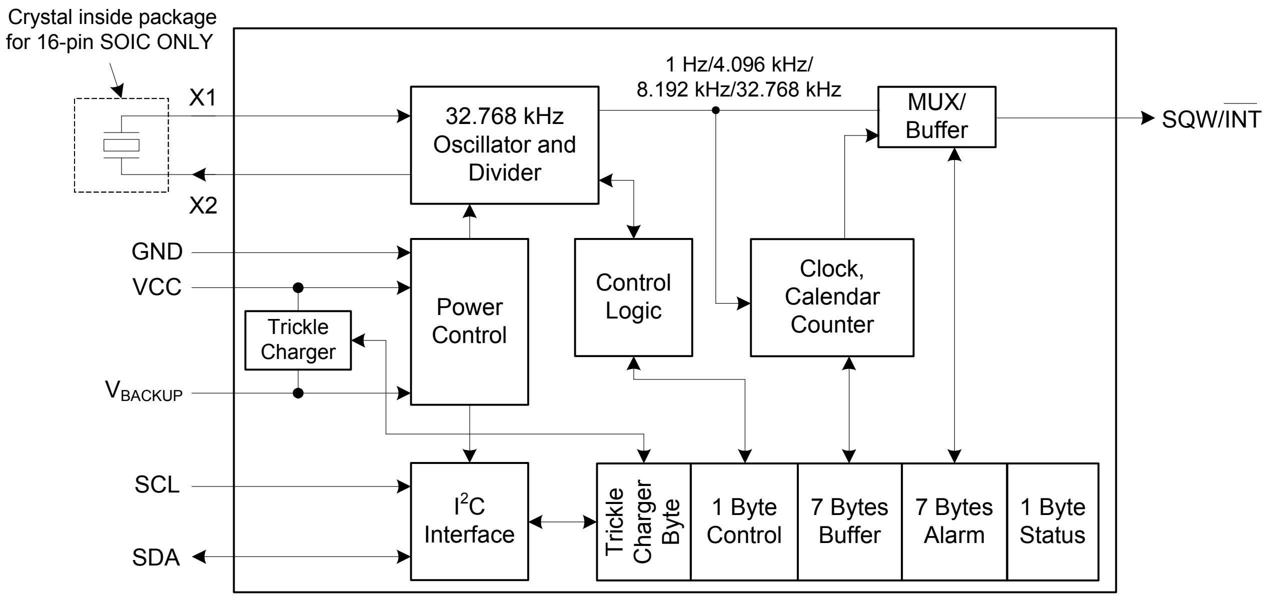
Applications

- Handhelds (GPS, POS terminals)
- Consumer Electronics (Set-Top Box, Digital Recording, Network Applications)
- Office (Fax/Printers, Copiers)
- Medical (Glucometer, Medicine Dispensers)
- Telecomm (Routers, Switches, Servers)
- Other (Thermostats, Vending Machines, Modems, Utility Meters)

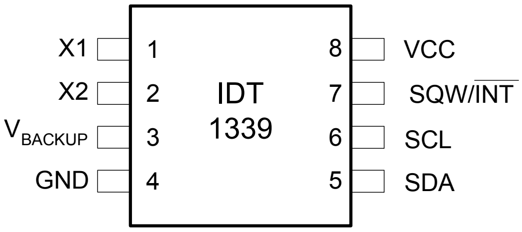
Features

- Real-Time Clock (RTC) counts seconds, minutes, hours, day, date, month, and year with leap-year compensation valid up to 2100
- Packaged in 8-pin MSOP, 8-pin SOIC, or 16-pin SOIC (surface-mount package with an integrated crystal)
- Fast mode I²C Serial interface
- Two time-of-day alarms
- Programmable square-wave output
- Oscillator stop flag
- Automatic power-fail detect and switch circuitry
- Trickle-charge capability
- Industrial temperature range (-40 to +85°C)
- Underwriters Laboratory (UL) recognized

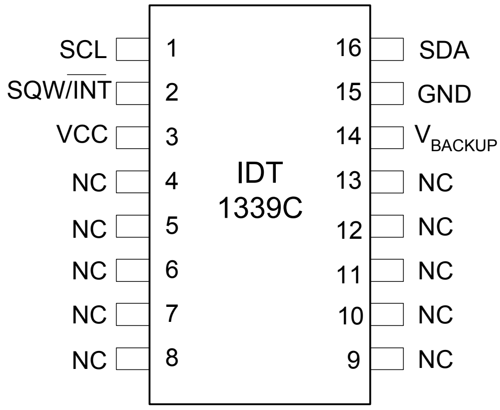
Block Diagram



Pin Assignment (8-pin MSOP/8-pin SOIC)



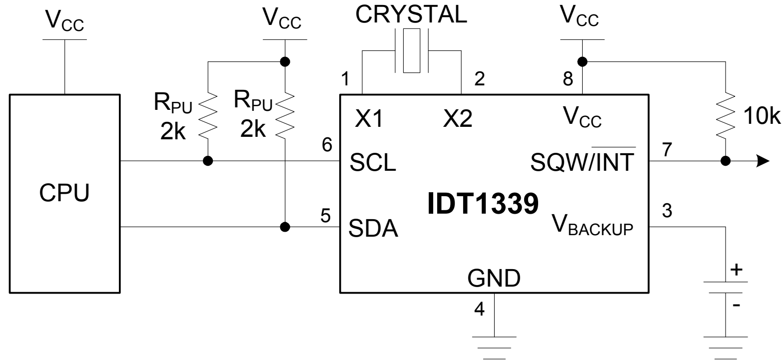
Pin Assignment (16-pin SOIC)



Pin Descriptions

Pin Number		Pin Name	Pin Description/Function
MSOP	SOIC		
1	—	X1	Connections for standard 32.768 kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 7 pF. An external 32.768 kHz oscillator can also drive the IDT1339. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is left floating.
2	—	X2	
3	14	V_{BACKUP}	Backup supply input. Supply voltage must be held between 1.3 V and 3.7 V for proper operation. This pin can be connected to a primary cell, such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap that can be charged using the trickle charger circuit. Diodes placed in series between the backup source and the VBAT pin may prevent proper operation. If a backup supply is not required, VBAT must be connected to ground. UL recognized to ensure against reverse charged current when used with a lithium cell.
4	15	GND	Connect to ground. DC power is provided to the device on these pins.
5	16	SDA	Serial data input/output. SDA is the input/output pin for the I²C serial interface. The SDA pin is an open-drain output and requires an external pull-up resistor (2 kΩ typical).
6	1	SCL	Serial clock input. SCL is used to synchronize data movement on the serial interface. It is an open-drain output and requires an external pull-up resistor (2 kΩ typical).
7	2	SQW/$\overline{INT}$	Square-Wave/Interrupt output. Programmable square-wave or interrupt output signal. The SQW/$\overline{INT}$ pin is an open-drain output and requires an external pull-up resistor (10 kΩ typical).
8	3	V_{CC}	Primary power supply. When voltage is applied within normal limits, the device is fully accessible and data can be written and read.
—	4 - 13	NC	No connect. These pins are unused and must be connected to ground.

Typical Operating Circuit



Detailed Description

The following sections discuss in detail the Oscillator block, Power Control block, Clock/Calendar Register, Alarms, trickle Charger, and Serial I²C block.

Oscillator Block

Selection of the right crystal, correct load capacitance and careful PCB layout are important for a stable crystal oscillator. Due to the optimization for the lowest possible current in the design for these oscillators, losses caused by parasitic currents can have a significant impact on the overall oscillator performance. Extra care needs to be taken to maintain a certain quality and cleanliness of the PCB.

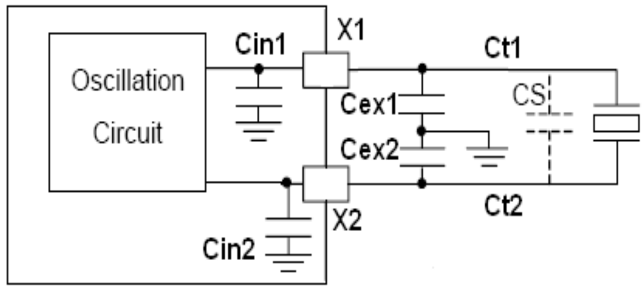
Crystal Selection

The key parameters when selecting a 32 kHz crystal to work with IDT1339 RTC are:

- Recommended Load Capacitance
- Crystal Effective Series Resistance (ESR)
- Frequency Tolerance

Effective Load Capacitance

Please see diagram below for effective load capacitance calculation. The effective load capacitance (CL) should match the recommended load capacitance of the crystal in order for the crystal to oscillate at its specified parallel resonant frequency with 0ppm frequency error.



$$CL = CS + ((CX1 * CX2) / (CX1 + CX2))$$
$$CX1 = (Cin1 + Cex1 + Ct1)$$
$$CX2 = (Cin2 + Cex2 + Ct2)$$

In the above figure, X1 and X2 are the crystal pins of our device. Cin1 and Cin2 are the internal capacitors which include the X1 and X2 pin capacitance. Cex1 and Cex2 are the external capacitors that are needed to tune the crystal frequency. Ct1 and Ct2 are the PCB trace capacitances between the crystal and the device pins. CS is the shunt capacitance of the crystal (as specified in the crystal manufacturer's datasheet or measured using a network analyzer).

Note: IDT1339CSRI integrates a standard 32.768 kHz (±20ppm) crystal in the package and contributes an additional frequency error of 10ppm at nominal V_{CC} (+3.3 V) and T_A=+25°C.

ESR (Effective Series Resistance)

Choose the crystal with lower ESR. A low ESR helps the crystal to start up and stabilize to the correct output frequency faster compared to high ESR crystals.

Frequency Tolerance

The frequency tolerance for 32kHz crystals should be specified at nominal temperature (+25°C) on the crystal manufacturer datasheet. The crystals used with IDT1339 typically have a frequency tolerance of ±20ppm at +25°C.

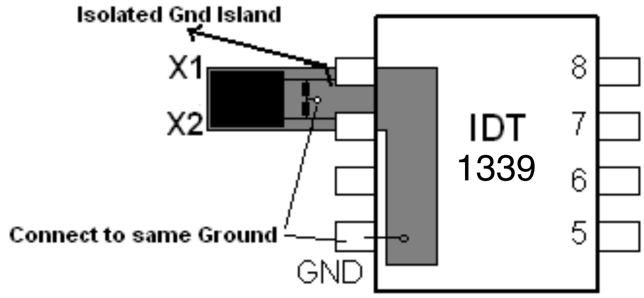
Specifications for a typical 32 kHz crystal used with our device are shown in the table below.

Parameter	Symbol	Min	Typ	Max	Units
Nominal Freq.	f_O		32.768		kHz
Series Resistance	ESR			50	kΩ
Load Capacitance	C_L		7		pF

PCB Design Consideration

- Signal traces between IDT device pins and the crystal must be kept as short as possible. This minimizes parasitic capacitance and sensitivity to crosstalk and EMI. Note that the trace capacitances play a role in the effective crystal load capacitance calculation.
- Data lines and frequently switching signal lines should be routed as far away from the crystal connections as possible. Crosstalk from these signals may disturb the oscillator signal.
- Reduce the parasitic capacitance between X1 and X2 signals by routing them as far apart as possible.
- The oscillation loop current flows between the crystal and the load capacitors. This signal path (crystal to CL1 to CL2 to crystal) should be kept as short as possible and ideally be symmetric. The ground connections for both capacitors should be as close together as possible. Never route the ground connection between the capacitors all around the crystal, because this long ground trace is sensitive to crosstalk and EMI.
- To reduce the radiation / coupling from oscillator circuit, an isolated ground island on the GND layer could be made. This ground island can be connected at one point to the GND layer. This helps to keep noise generated by the oscillator circuit locally on this separated island. The ground connections for the load capacitors and the oscillator should be connected to this island.

PCB Layout



PCB Assembly, Soldering and Cleaning

Board-assembly production process and assembly quality can affect the performance of the 32 kHz oscillator. Depending on the flux material used, the soldering process can leave critical residues on the PCB surface. High humidity and fast temperature cycles that cause humidity condensation on the printed circuit board can create process residuals. These process residuals cause the insulation of the sensitive oscillator signal lines towards each other and neighboring signals on the PCB to decrease. High humidity can lead to moisture condensation on the surface of the PCB and, together with process residuals, reduce the surface resistivity of the board. Flux residuals on the board can cause leakage current paths, especially in humid environments. Thorough PCB cleaning is therefore highly recommended in order to achieve maximum performance by removing flux residuals from the board after assembly. In general, reduction of losses in the oscillator circuit leads to better safety margin and reliability.

Power Control

The power-control function is provided by a precise, temperature-compensated voltage reference and a comparator circuit that monitors the V_{CC} level. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. The registers are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels (Table 1). After V_{CC} returns above V_{PF}, read and write access is allowed after t_{REC} (see the "Power-Up/Down Timing" diagram).

Table 1. Power Control

Supply Condition	Read/Write Access	Powered By
$V_{CC} < V_{PF}$, $V_{CC} < V_{BACKUP}$	No	V_{BACKUP}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BACKUP}$	No	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BACKUP}$	Yes	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BACKUP}$	Yes	V_{CC}

Power-up/down Timing

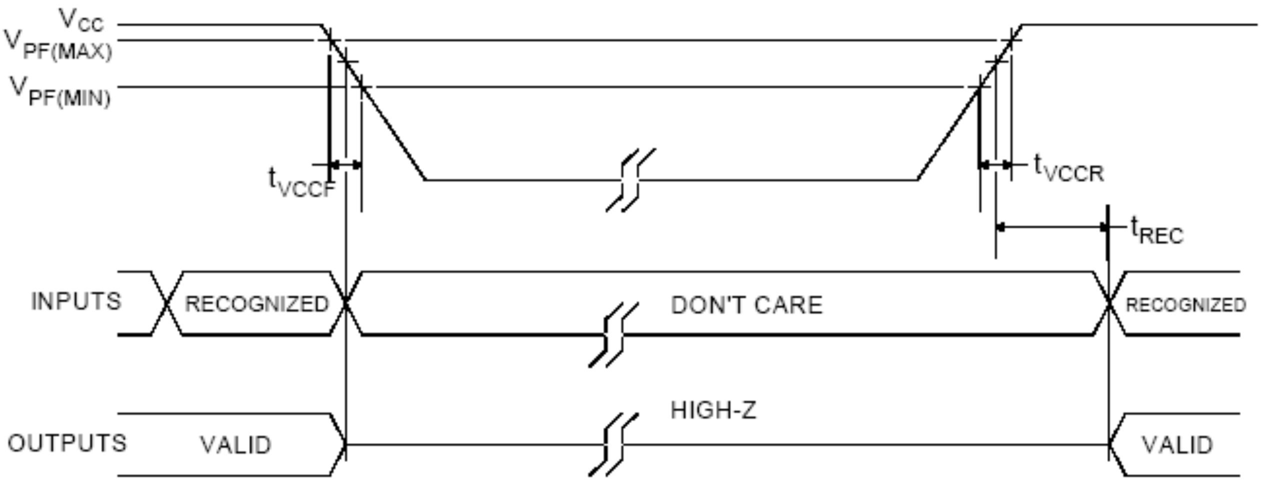


Table 2. Power-up/down Characteristics

Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Recovery at Power-up	t_{REC}	(see note 1)			2	ms
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_{VCCF}	(see note 2)	3			ms
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_{VCCR}		0			µs

Note 1: This delay applies only if the oscillator is running. If the oscillator is disabled or stopped, no power-up delay occurs.

Note 2: Measured at typ VBAT level.

Address Map

Table 3 (Timekeeper Registers) shows the address map for the IDT1339 registers. During a multibyte access, when the address pointer reaches the end of the register space (10h), it wraps around to location 00h. On an I^2C START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Table 3. Timekeeper Registers

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function	Range
00h	0	10 seconds			Seconds				Seconds	00 - 59
01h	0	10 minutes			Minutes				Minutes	00 - 59
02h	0	12/$\overline{24}$	$\overline{AM}$/PM 10 hour	10 hour	Hour				Hours	1 - 12 + AM/PM 00 - 23
03h	0	0	0	0	0	Day			Day	1 - 7
04h	0	0	10 date		Date				Date	01 - 31
05h	Century	0	0	10 month	Month				Month/Century	01 - 12 + Century
06h	10 year				Year				Year	00 - 99
07h	A1M1	10 seconds			Seconds				Alarm 1 Seconds	00 - 59
08h	A1M2	10 minutes			Minutes				Alarm 1 Minutes	00 - 59
09h	A1M3	12/$\overline{24}$	$\overline{AM}$/PM 10 hour	10 hour	Hour				Alarm 1 Hours	1 - 12 + AM/PM 00 - 23
0Ah	A1M4	DY/DT	10 date		Day, Date				Alarm 1 Day, Alarm 1 Date	1 - 7, 1 - 31
0Bh	A2M2	10 minutes			Minutes				Alarm 2 Minutes	00 - 59
0Ch	A2M3	12/$\overline{24}$	$\overline{AM}$/PM 10 hour	10 hour	Hour				Alarm 2 Hours	1 - 12 + AM/PM 00 - 23
0Dh	A2M4	DY/$\overline{DT}$	10 date		Day, Date				Alarm 2 Day, Alarm 2 Date	1 - 7, 1 - 31
0Eh	$\overline{EOSC}$	0	BBSQI	RS2	RS1	INTCN	A2IE	A1IE	Control	
0Fh	OSF	0	0	0	0	0	A2F	A1F	Status	
10h	TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	Trickle Charger	

Note: Unless otherwise specified, the state of the registers are not defined when power is first applied or when V_{CC} and V_{BACKUP} falls below the $V_{BACKUP(min)}$.

Time and Date Operation

The time and date information is obtained by reading the appropriate register bytes. Table 3 shows the RTC registers. The time and date are set or initialized by writing the appropriate register bytes. The contents of the time and date registers are in the BCD format. The IDT1339 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{\text{AM}}$/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20 to 23 hours). All hours values, including the alarms, must be re-entered whenever the 12/$\overline{\text{24}}$-hour mode bit is changed. The century bit (bit 7 of the month register) is toggled when the years register overflows from 99 to 00. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined, but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any start or stop, and when the address pointer rolls over to zero. The countdown chain is reset whenever the seconds register is written. Write transfers occurs on the acknowledge pulse from the device. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within one second. If enabled, the 1 Hz square-wave output transitions high 500 ms after the seconds data transfer, provided the oscillator is already running.

Alarms

The IDT1339 contains two time of day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh. The alarms can be programmed (by the Alarm Enable and INTCN bits of the Control Register) to activate the SQW/$\overline{\text{INT}}$ output on an alarm match condition. Bit 7 of each of the time of day/date alarm registers are mask bits (Table 4). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h to 06h match the values stored in the time of day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 4 shows the possible settings. Configurations not listed in the table result in illogical operation.

The DY/$\overline{\text{DT}}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/$\overline{\text{DT}}$ is written to a logic 0, the alarm is the result of a match with date of the month. If DY/$\overline{\text{DT}}$ is written to a logic 1, the alarm is the result of a match with day of the week.

The device checks for an alarm match once per second. When the RTC register values match alarm register settings, the corresponding Alarm Flag 'A1F' or 'A2F' bit is set to logic 1. If the corresponding Alarm Interrupt Enable 'A1IE' or 'A2IE' is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition activates the SQW/$\overline{\text{INT}}$ signal. If the BBSQI bit is set to 1, the $\overline{\text{INT}}$ output activates while the part is being powered by V_{BACKUP}. The alarm output remains active until the alarm flag is cleared by the user.

Table 4. Alarm Mask Bits

DY/$\overline{DT}$	Alarm 1 Register Mask Bits (Bit 7)				Alarm Rate
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second.
X	1	1	1	0	Alarm when seconds match.
X	1	1	0	0	Alarm when minutes and seconds match.
X	1	0	0	0	Alarm when hours, minutes, and seconds match.
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match.
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match.
DY/$\overline{DT}$	**Alarm 2 Register Mask Bits (Bit 7)**				**Alarm Rate**
	A2M4	**A2M3**	**A2M2**		
X	1	1	1		Alarm once per minute (00 sec. of every min.).
X	1	1	0		Alarm when minutes match.
X	1	0	0		Alarm when hours and minutes match.
0	0	0	0		Alarm when date, hours, and minutes match.
1	0	0	0		Alarm when day, hours, and minutes match.

Special-Purpose Registers

The IDT1339 has two additional registers (control and status) that control the RTC, alarms, and square-wave output.

Control Register (0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{\text{EOSC}}$	0	BBSQI	RS2	RS1	INTCN	A2IE	A1IE

Bit 7: Enable Oscillator ($\overline{\text{EOSC}}$). This bit when set to logic 0 starts the oscillator. When this bit is set to a logic 1, the oscillator is stopped. This bit is enabled (logic 0) when power is first applied.

Bit 5: Battery-Backed Square-Wave and Interrupt Enable (BBSQI). This bit when set to a logic 1 enables the square wave or interrupt output when V_{CC} is absent and the IDT1339 is being powered by the V_{BACKUP} pin. When BBSQI is a logic 0, the SQW/$\overline{\text{INT}}$ pin goes high impedance when V_{CC} falls below the power-fail trip point. This bit is disabled (logic 0) when power is first applied.

Bits 4 and 3: Rate Select (RS2 and RS1). These bits control the frequency of the square-wave output when the square wave has been enabled. Table 5 shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (32 kHz) when power is first applied.

Table 5. SQW/$\overline{\text{INT}}$ Output

INTCN	RS2	RS1	SQW/$\overline{\text{INT}}$ Output	A2IE	A1IE
0	0	0	1 Hz	X	X
0	0	1	4.096 kHz	X	X
0	1	0	8.192 kHz	X	X
0	1	1	32.768 kHz	X	X
1	X	X	$\overline{\text{A1F}}$	0	1
1	X	X	$\overline{\text{A2F}}$	1	0
1	X	X	$\overline{\text{A2F}} + \overline{\text{A1F}}$	1	1

Bit 2: Interrupt Control (INTCN). This bit controls the relationship between the two alarms and the interrupt output pins. When the INTCN bit is set to logic 1, a match between the timekeeping registers and the alarm 1 or alarm 2 registers activate the SQW/$\overline{\text{INT}}$ pin (provided that the alarm is enabled). When the INTCN bit is set to logic 0, a square wave is output on the SQW/$\overline{\text{INT}}$ pin. This bit is set to logic 0 when power is first applied.

Bit 1: Alarm 2 Interrupt Enable (A2IE). When set to a logic 1, this bit permits the Alarm 2 Flag (A2F) bit in the status register to assert SQW/$\overline{\text{INT}}$ (when INTCN = 1). When the A2IE bit is set to logic 0 or INTCN is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Bit 0: Alarm 1 Interrupt Enable (A1IE). When set to logic 1, this bit permits the Alarm 1 Flag (A1F) bit in the status register to assert SQW/$\overline{\text{INT}}$ (when INTCN = 1). When the A1IE bit is set to logic 0 or INTCN is set to logic 0, the A1F bit does not initiate an interrupt signal. The A1IE bit is disabled (logic 0) when power is first applied.

Status Register (0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSF	0	0	0	0	0	A2F	A1F

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and date data. This bit is edge triggered and is set to logic 1 when the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.

2) The voltage on both V_{CC} and V_{BACKUP} are insufficient to support oscillation.

3) The $\overline{\text{EOSC}}$ bit is turned off.

4) External influences on the crystal (e.g., noise, leakage, etc.).

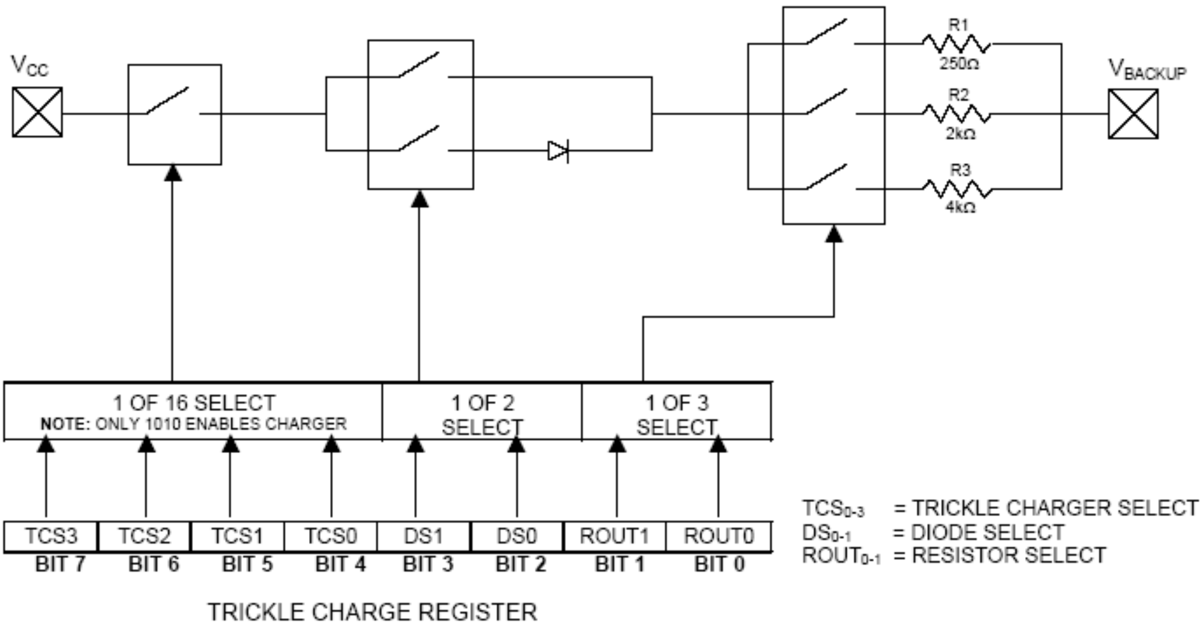
This bit remains at logic 1 until written to logic 0. This bit can only be written to a logic 0.

Bit 1: Alarm 2 Flag (A2F). A logic 1 in the Alarm 2 Flag bit indicates that the time matched the alarm 2 registers. If the A2IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/$\overline{\text{INT}}$ pin is also asserted. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Bit 0: Alarm 1 Flag (A1F). A logic 1 in the Alarm 1 Flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/$\overline{\text{INT}}$ pin is also asserted. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Trickle Charger Register (10h)

Programmable Trickle Charger



The simplified "Programmable Trickle Charger" schematic shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4 to 7) control the selection of the trickle charger. To prevent accidental enabling, only a pattern of 1010 on the TCS bits enables the trickle charger. All other patterns disable the trickle charger. The trickle charger is disabled when power is first applied. The diode-select (DS) bits (bits 2 and 3) select whether or not a diode is connected between V_{CC} and V_{BACKUP}. The ROUT bits (bits 0 and 1) select the value of the resistor connected between V_{CC} and V_{BACKUP}. Table 6 shows the bit values.

Table 6. Trickle Charger Register (10h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function
TCS3	**TCS2**	**TCS1**	**TCS0**	**DS1**	**DS0**	**ROUT 1**	**ROUT 0**	
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
X	X	X	X	X	X	0	0	Disabled
1	0	1	0	0	1	0	1	No diode, 250Ω resistor
1	0	1	0	1	0	0	1	One diode, 250Ω resistor
1	0	1	0	0	1	1	0	No diode, 2kΩ resistor
1	0	1	0	1	0	1	0	One diode, 2kΩ resistor
1	0	1	0	0	1	1	1	No diode, 4kΩ resistor
1	0	1	0	1	0	1	1	One diode, 4kΩ resistor
0	0	0	0	0	0	0	0	Initial power-up values

Warning: The ROUT value of 250Ω must not be selected whenever V_{CC} is greater than 3.63 V.

The user determines diode and resistor selection according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a 3.3 V system power supply is applied to V_{CC} and a super cap is connected to V_{BACKUP}. Also assume that the trickle charger has been enabled with a diode and resistor R2 between V_{CC} and V_{BACKUP}. The maximum current I_{MAX} would therefore be calculated as follows:

$$I_{MAX} = (3.3\text{ V} - \text{diode drop}) / R2 \approx (3.3\text{ V} - 0.7\text{ V}) / 2k\Omega \approx 1.3\text{ mA}$$

As the super cap or battery charges, the voltage drop between V_{CC} and V_{BACKUP} decreases and therefore the charge current decreases.

I^{2}C Serial Data Bus

The IDT1339 supports the I^{2}C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The IDT1339 operates as a slave on the I^{2}C bus. Within the bus specifications, a standard mode (100 kHz cycle rate) and a fast mode (400 kHz cycle rate) are defined. The IDT1339 works in both modes. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (see the “Data Transfer on I^{2}C Serial Bus” figure):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

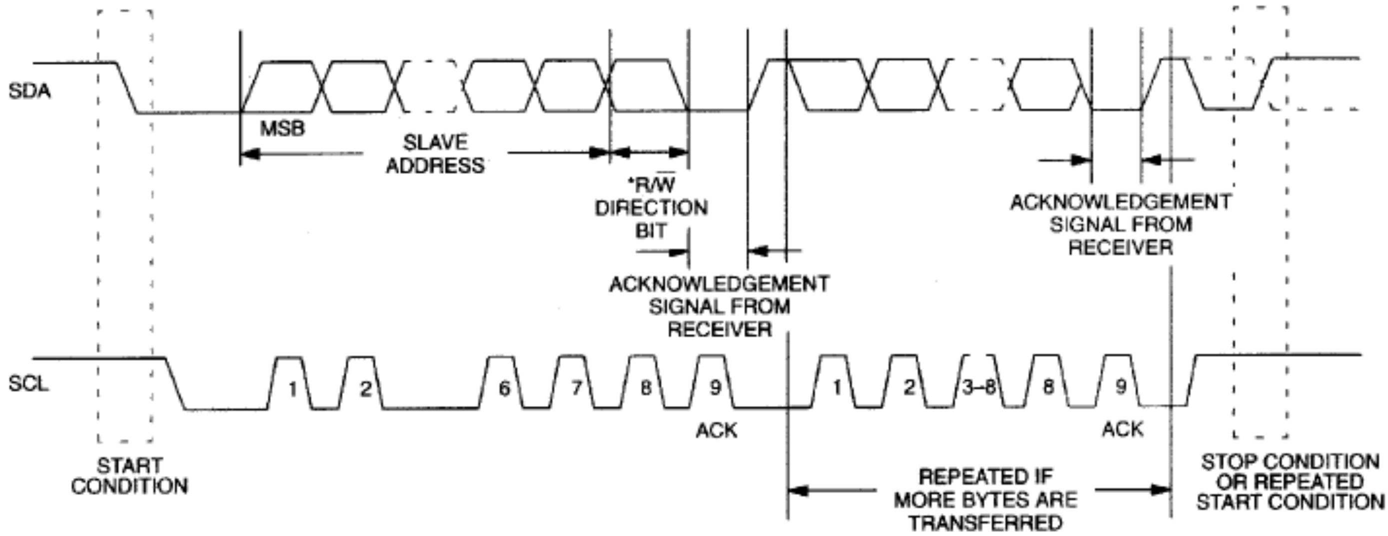
Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Timeout: Timeout is where a slave device resets its interface whenever Clock goes low for longer than the timeout, which is typically 35mSec. This added logic deals with slave errors and recovering from those errors. When timeout occurs, the slave interface should re-initialize itself and be ready to receive a communication from the master, but it will expect a Start prior to any new communication.

Data Transfer on I²C Serial Bus



Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2) **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. This is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a "not acknowledge" is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

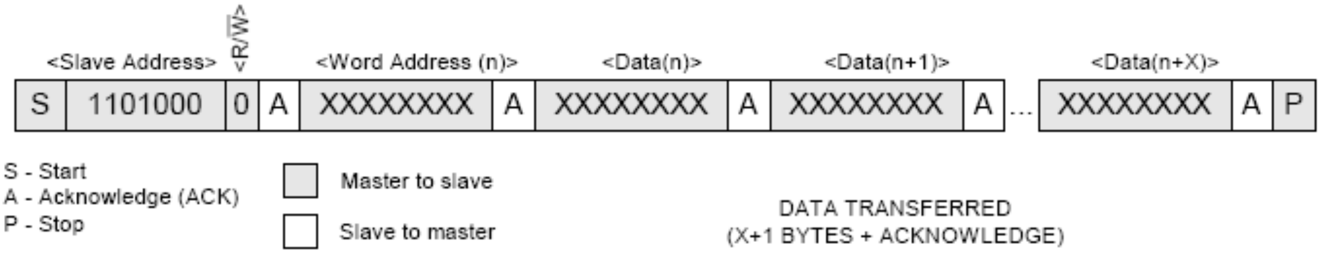
The IDT1339 can operate in the following two modes:

1) **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see the "Data Write–Slave Receiver Mode" figure). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit IDT1339 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 0 for a write. After receiving and decoding the slave address byte the slave outputs an acknowledge on the SDA line. After the IDT1339 acknowledges the slave address + write bit, the master transmits a register address to the IDT1339. This sets the register pointer on the IDT1339, with the IDT1339 acknowledging the transfer. The master may then transmit zero or more bytes of data, with the IDT1339 acknowledging each byte received. The address pointer increments after each data byte is transferred. The master generates a STOP condition to terminate the data write.

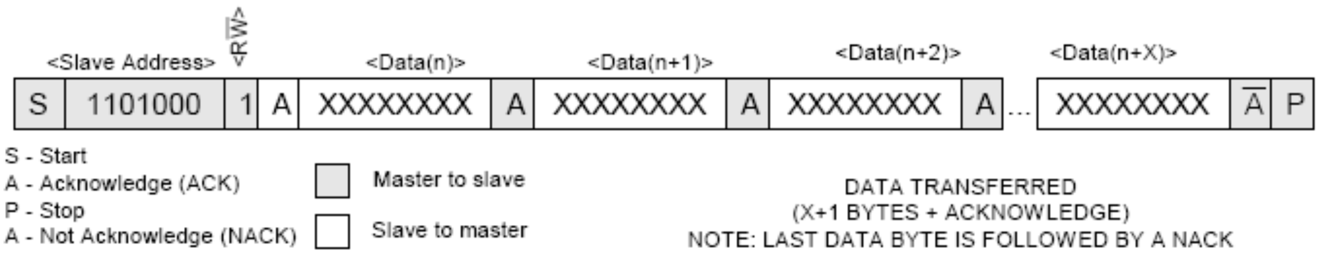
2) **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the IDT1339 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (see the "Data Read–Slave Transmitter Mode" figure). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit IDT1339 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 1 for a read. After receiving and decoding the slave address byte the slave outputs an acknowledge on the SDA line. The IDT1339 then begins to transmit data starting with the register address pointed to by

the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The address pointer is incremented after each byte is transferred. The IDT1339 must receive a “not acknowledge” to end a read.

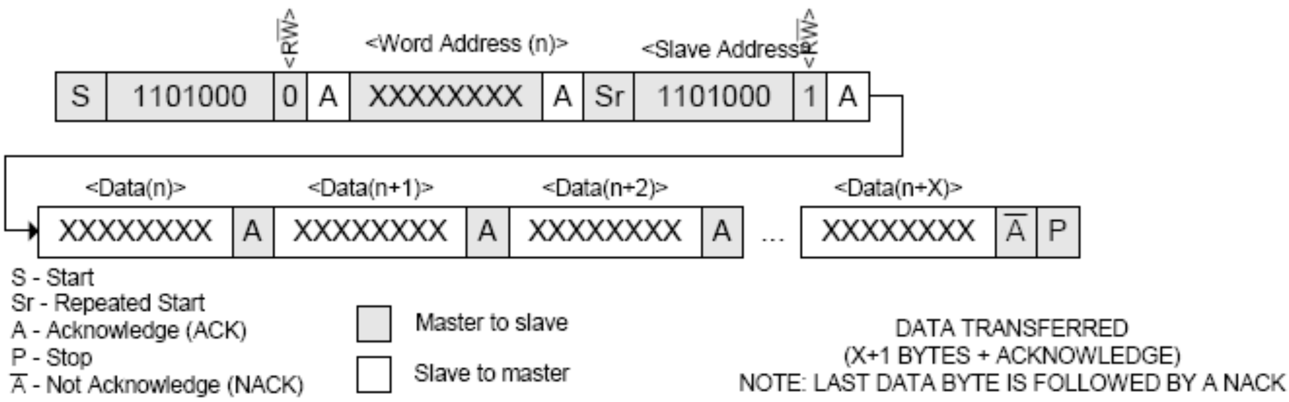
Data Write – Slave Receiver Mode



Data Read (from current Pointer location) – Slave Transmitter Mode



Data Read (Write Pointer, then Read) – Slave Receive and Transmit



Handling, PCB Layout, and Assembly

The IDT1339 package contains a quartz tuning-fork crystal. Pick-and-place equipment may be used, but precautions should be taken to ensure that excessive shocks are avioded. Ultarsonic cleaning equipment should be avioded to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All NC (no connect) pins must be connected to ground.

Moisture-sensitive packages are shipped from the factory dry-packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT1339. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Symbol	Rating
All Inputs and Outputs		-0.3 V to +6.0 V
Storage Temperature		-55 to +125°C
Soldering Temperature		260°C

Recommended DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Ambient Operating Temperature	T_A	-40		+85	°C
Backup Supply Voltage	V_{BACKUP}	1.3	3.0	3.7	V
Pull-up Resistor Voltage (SQW/$\overline{INT}$, SDA, SCL), V_{CC} = 0V	V_{PU}			5.5	V
Logic 1	V_{IH}	$0.8V_{CC}$		V_{CC} + 0.3	V
Logic 0	V_{IL}	-0.3		$0.2V_{CC}$	V
Supply Voltage					
IDT1339-2, Note A	V_{CC}	V_{PF}	2.0	5.5	V
IDT1339-31, Note A		V_{PF}	3.3	5.5	
Power Fail Voltage					
IDT1339-2, Note B	V_{PF}	1.40	1.70	1.80	V
IDT1339-31, Note B		2.45	2.70	2.97	

Note A: Operating voltages without a back up supply connected.

Note B: When a back up supply voltage is connected choose proper part number 1339-2 or 1339-31 depending upon the back up supply voltage.

DC Electrical Characteristics

Unless stated otherwise, **V_{CC} = MIN to MAX**, Ambient Temperature -40 to +85°C, Note 1

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Leakage	I_{LI}	Note 2			1	µA
I/O Leakage	I_{LO}	Note 3			1	µA
Logic 0 Out $V_{CC} \geq 2.0$ V	I_{OL}	IDT1339-2, Note 3			3	mA
Logic 0 Out VOL = 0.4; VCC > VCC Min. $V_{CC} \geq 2.0$ V	I_{OL}	IDT1339-31, Note 3			3	mA
Logic 0 Out VOL = 0.2 V (V_{CC}); 1.8 V < V_{CC} < 2.0 V	I_{OL}	Note 3			3	mA
Logic 0 Out VOL = 0.2 V (V_{CC}); 1.3 V < V_{CC} < 1.8 V	I_{OL}	Note 3			250	µA
V_{CC} Active Current	I_{CCA}	Note 4			450	µA
V_{CC} Standby Current, Note 5	I_{CCS}	$V_{CC} \leq 3.63$ V		80	150	µA
		3.63 V < $V_{CC} \leq 5.5$ V			200	
Trickle-charger Resistor Register 10h = A5h, V_{CC} = Typ, V_{BACKUP} = 0V	R1	Note 6		250		Ω
Trickle-charger Resistor Register 10h = A6h, V_{CC} = Typ, V_{BACKUP} = 0V	R2			2000		Ω
Trickle-charger Resistor Register 10h = A7h, V_{CC} = Typ, V_{BACKUP} = 0V	R3			4000		Ω
V_{BACKUP} Leakage Current	I_{BKLKG}			25	100	nA

DC Electrical Characteristics

Unless stated otherwise, **V_{CC} = 0V**, Ambient Temperature -40 to +85°C, Note 1

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
V_{BACKUP} Current $\overline{EOSC}$ = 0, SQW Off	I_{BKOSC}	Note 7		800	1200	nA
V_{BACKUP} Current $\overline{EOSC}$ = 0, SQW On	I_{BKSQW}	Note 7		1025	1400	nA
V_{BACKUP} Current $\overline{EOSC}$ = 1	I_{BKDR}	Note 7		120	300	nA

AC Electrical Characteristics

Unless stated otherwise, **V_{CC} = MIN to MAX**, Ambient Temperature -40 to +85°C, Note 13

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
SCL Clock Frequency	f_{SCL}	Fast Mode	100		400	kHz
		Standard Mode			100	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast Mode	1.3			µs
		Standard Mode	4.7			
Hold Time (Repeated) START Condition, Note 8	$t_{HD:STA}$	Fast Mode	0.6			µs
		Standard Mode	4.0			
Low Period of SCL Clock	t_{LOW}	Fast Mode	1.3			µs
		Standard Mode	4.7			
High Period of SCL Clock	t_{HIGH}	Fast Mode	0.6			µs
		Standard Mode	4.0			
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast Mode	0.6			µs
		Standard Mode	4.7			
Data Hold Time, Notes 9, 10	$t_{HD:DAT}$	Fast Mode	0		0.9	µs
		Standard Mode	0			
Data Setup Time, Note 11	$t_{SU:DAT}$	Fast Mode	100			ns
		Standard Mode	250			
Rise Time of Both SDA and SCL Signals, Note 12	t_R	Fast Mode	$20 + 0.1C_B$		300	ns
		Standard Mode	$20 + 0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals, Note 12	t_F	Fast Mode	$20 + 0.1C_B$		300	ns
		Standard Mode	$20 + 0.1C_B$		300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast Mode	0.6			µs
		Standard Mode	4.0			
Capacitive Load for Each Bus Line, Note 12	C_B				400	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$	Note 13			10	pF
Oscillator Stop Flag (OSF) Delay	t_{OSF}	Note 14		100		ms

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.

Note 1: Limits at -40°C are guaranteed by design and are not production tested.

Note 2: SCL only.

Note 3: SDA and SQW/$\overline{\text{INT}}$.

Note 4: I_{CCA}—SCL at f_{SC} max, VIL = 0.0V, VIH = V_{CC}, trickle charger disabled.

Note 5: Specified with the I²C bus inactive, VIL = 0.0V, VIH = V_{CC}, trickle charger disabled.

Note 6: V_{CC} must be less than 3.63 V if the 250Ω resistor is selected.

Note 7: Using recommended crystal on X1 and X2.

Note 8: After this period, the first clock pulse is generated.

Note 9: A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 10: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

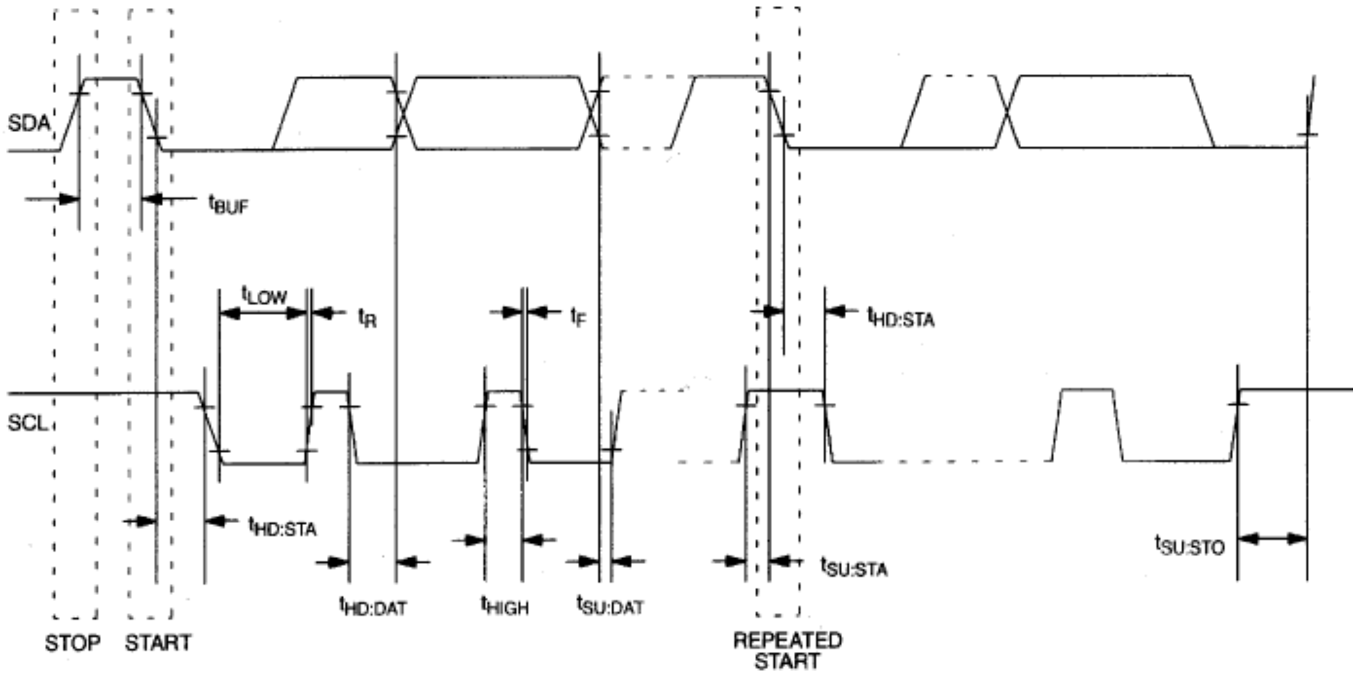
Note 11: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq$ to 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R(MAX)} + t_{SU:DAT} = 1000 + 250 = 1250$ ns before the SCL line is released.

Note 12: C_B—total capacitance of one bus line in pF.

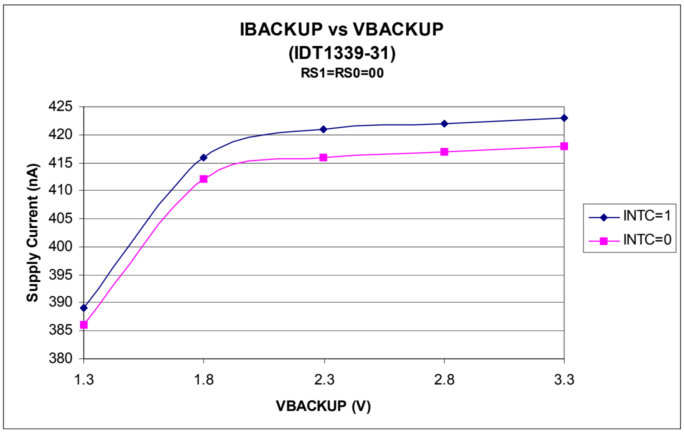
Note 13: Guaranteed by design. Not production tested.

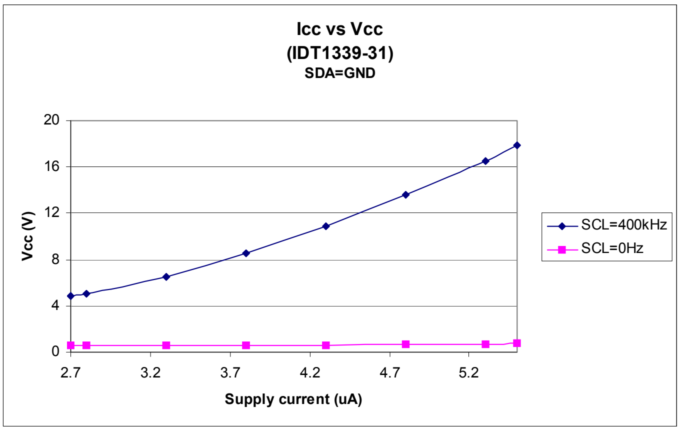
Note 14: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over the voltage range of $0.0V \leq V_{CC} \leq V_{CC}MAX$ and $1.3\ V \leq V_{BACKUP} \leq 3.7\ V$.

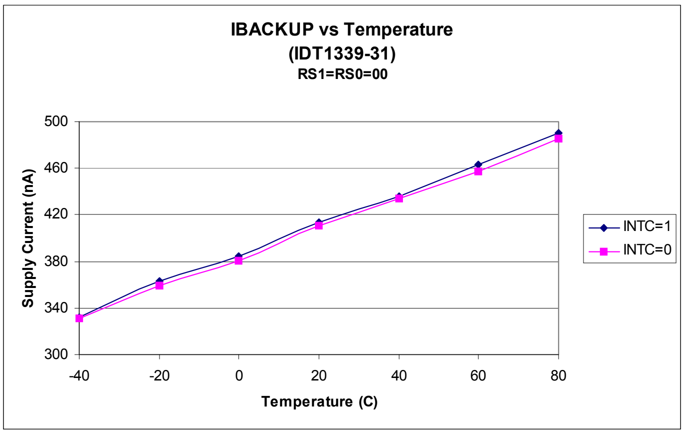
Timing Diagram

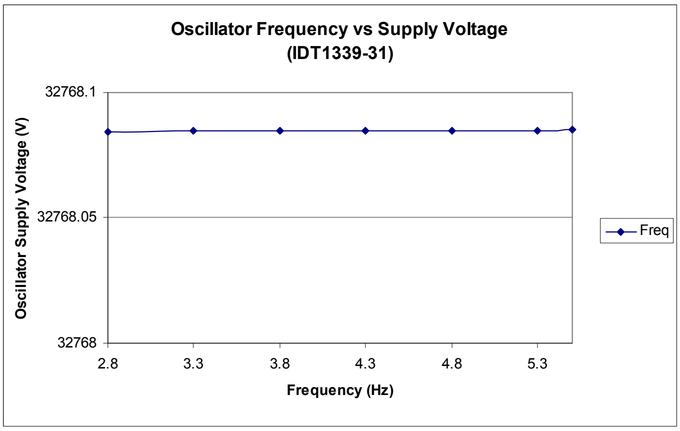


Typical Operating Characteristics (V_{CC}=3.3V, T_A=25°C)









Thermal Characteristics for 8MSOP

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		95		°C/W
Thermal Resistance Junction to Case	θ_{JC}			48		°C/W

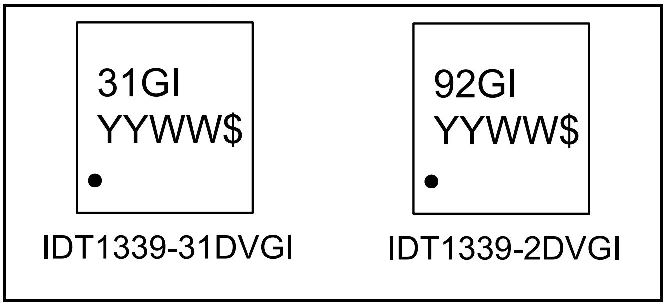
Thermal Characteristics for 8SOIC

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

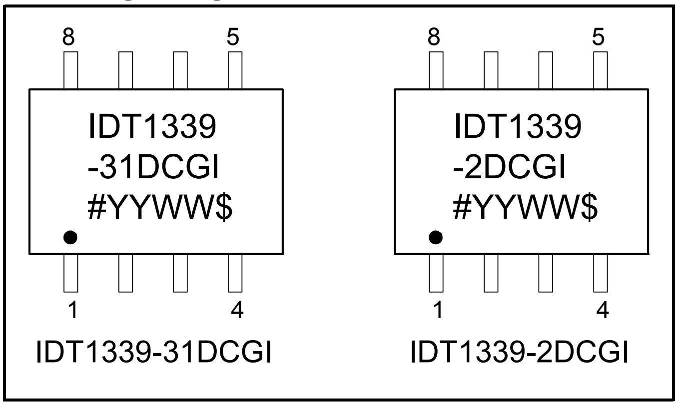
Thermal Characteristics for 16SOIC

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		115		°C/W
	θ_{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ_{JC}			58		°C/W

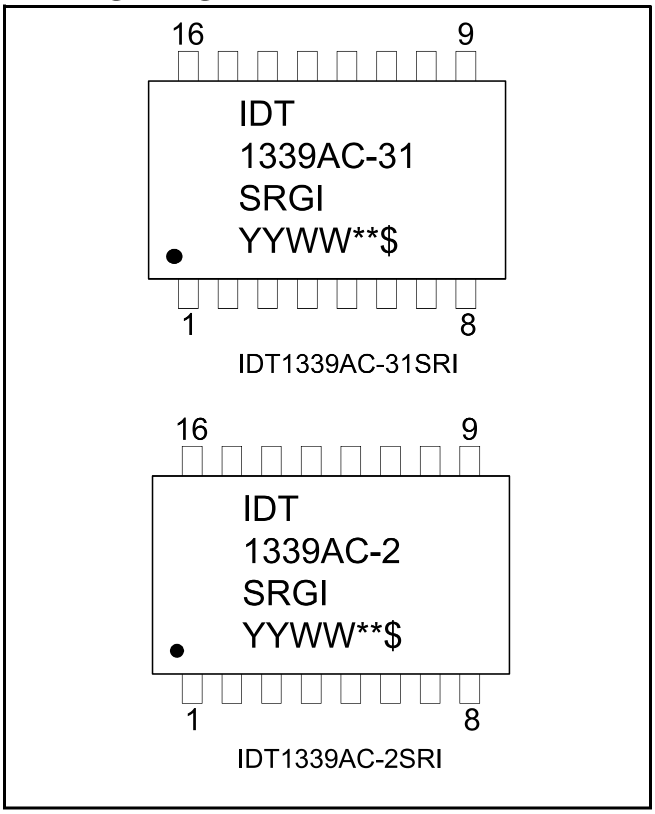
Marking Diagram (8 MSOP)



Marking Diagram (8 SOIC)



Marking Diagram (16 SOIC)

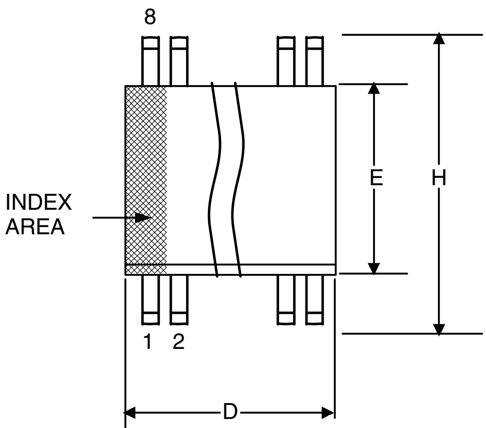


Notes:

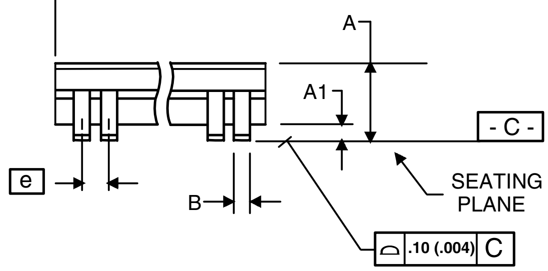
1. '#' is the lot number.
2. '$' is the assembly mark code.
3. '**' is the lot sequence.
4. YYWW is the last two digits of the year and week that the part was assembled.
5. "G" denotes RoHS compliant package.
6. "I" denotes industrial grade.
7. Bottom marking: country of origin if not USA.

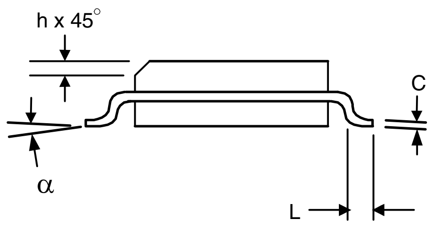
Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



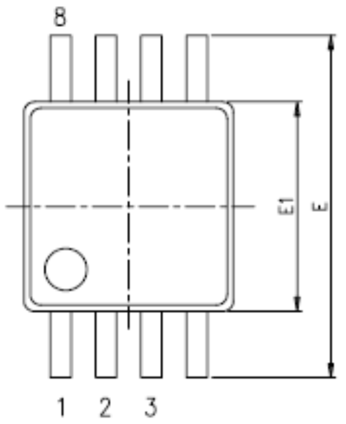
	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

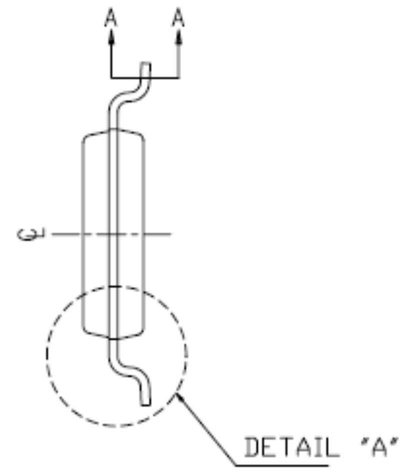


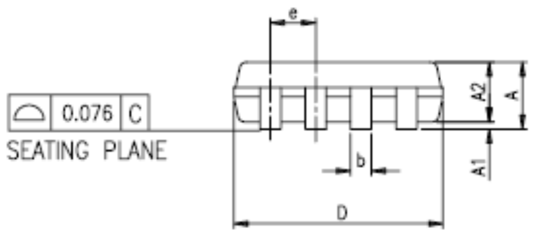


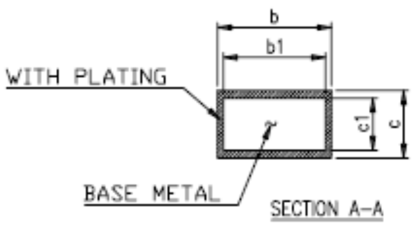
Package Outline and Package Dimensions (8-pin MSOP, 3.00 mm Body)

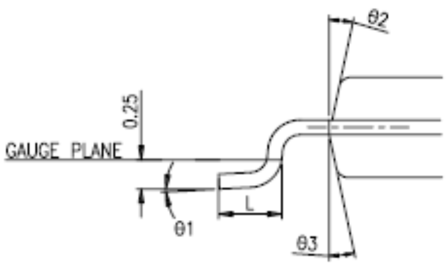
Package dimensions are kept current with JEDEC Publication No. 95









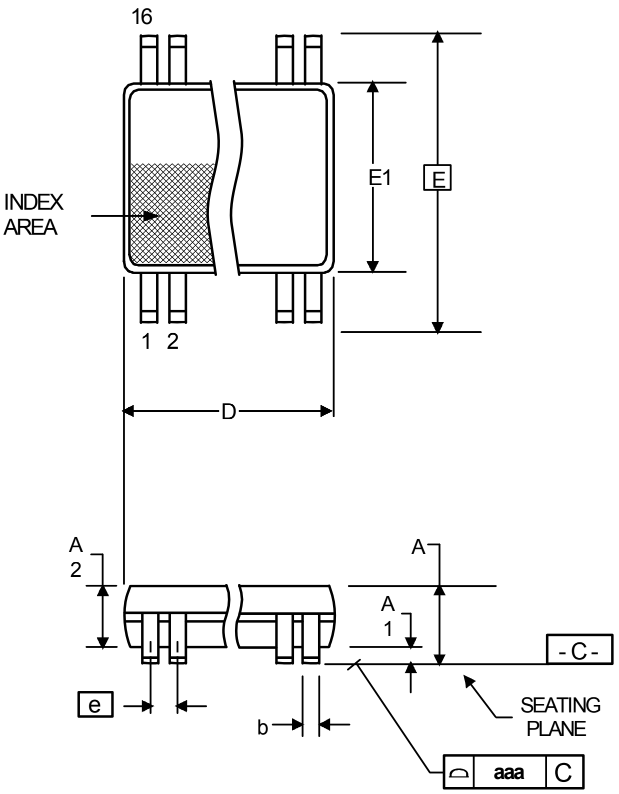


	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.10	--	0.043
A1	0.05	0.15	0.002	0.006
A2	0.81	0.91	0.032	0.036
b	0.22	0.38	0.008	0.015
b1	0.22	0.33	0.008	0.013
c	0.13	0.18	0.005	0.009
c1	0.13	0.18	0.005	0.007
D	2.90	3.10	0.114	0.122
E	4.90 BASIC		0.193 BASIC	
E1	2.90	3.10	0.114	0.122
e	0.65 Basic		0.0256 Basic	
L	0.445	0.648	0.0175	0.0255
Θ1	0°	6°	0°	6°

*For reference only. Controlling dimensions in mm.
"E" dimension is 4.9mm Basic per JEDEC standard; Tolerance is ±0.25mm or ±0.0098 inches

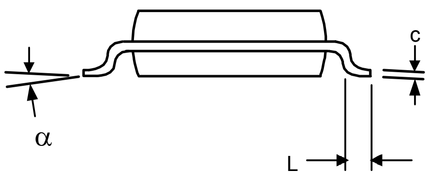
Package Outline and Package Dimensions (16-pin SOIC, 300 mil Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	Min	Max	Min	Max
A	--	2.65	--	0.104
A1	0.10	--	0.0040	--
A2	2.05	2.55	0.081	0.100
b	0.33	0.51	0.013	0.020
c	0.18	0.32	0.007	0.013
D	10.10	10.50	0.397	0.413
E	10.00	10.65	0.394	0.419
E1	7.40	7.60	0.291	0.299
e	1.27 Basic		0.050 Basic	
L	0.40	1.27	0.016	0.050
α	0°	8°	0°	8°
aaa	-	0.10	-	0.004

*For reference only. Controlling dimensions in mm.



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
1339-2DVGI	see page 20	Tubes	8-pin MSOP	-40 to +85° C
1339-2DVGI8		Tape and Reel	8-pin MSOP	-40 to +85° C
1339-2DCGI		Tubes	8-pin SOIC	-40 to +85° C
1339-2DCGI8		Tape and Reel	8-pin SOIC	-40 to +85° C
1339AC-2SRGI		Tubes	16-pin SOIC	-40 to +85° C
1339AC-2SRGI8		Tape and Reel	16-pin SOIC	-40 to +85° C
1339-31DVGI		Tubes	8-pin MSOP	-40 to +85° C
1339-31DVGI8		Tape and Reel	8-pin MSOP	-40 to +85° C
1339-31DCGI		Tubes	8-pin SOIC	-40 to +85° C
1339-31DCGI8		Tape and Reel	8-pin SOIC	-40 to +85° C
1339AC-31SRGI		Tubes	16-pin SOIC	-40 to +85° C
1339AC-31SRGI8		Tape and Reel	16-pin SOIC	-40 to +85° C

The IDT1339 packages are RoHS compliant. Packages without the integrated crystal are Pb-free; packages that include the integrated crystal (as designated with a “C” before the dash number) may include lead that is exempt under RoHS requirements. The lead finish is JESD91 category e3.

“A” is the device revision designator and will not correlate to the datasheet revision.

Revision History

Rev.	Date	Originator	Description of Change
A	06/26/07	S. Sharma	New device. Preliminary release.
B	11/01/07	J. Sarma	Updated ordering info for 16-pin SOIC package.
C	01/17/08	J. Sarma	Added 8-pin SOIC package; updated “Power-up/down Characteristics” table; updates to “Absolute Maximum Ratings” table.
D	02/11/08	J. Sarma	Combined part numbers for 1339-3 and 1339-33 into one part number: 1339-31.
E	03/28/08	J.Sarma	Added new note to Part Ordering information pertaining to RoHS compliance and Pb-free devices.
F	05/18/08	J.Sarma	Changed the part number for the 16PIN SOIC package from IDT1339C-31SOGI to IDT1339C-31SRI and the IDT1339C-2SOGI changed to IDT1339C-2SRI
G	08/04/08	J.Sarma	Removed “Preliminary”; removed UL statement from pin 3 description.
H	11/20/08	J.Sarma	Updated Block Diagram, Detailed description section(s), Operating Circuit diagram, and Typical Operating Characteristics diagrams.
I	12/03/08	J.Sarma	Updated Block Diagram, Features bullets, Pin descriptions, Typical Operating Characteristics diagrams; added marking diagrams.
J	11/10/09		Added “Handling, PCB Layout, and Assembly” section.
K	03/29/10	S.S.	Added “Timeout” paragraph on page 11.
L	7/30/10	L.P.	Added Underwriters Laboratory recognition.
M	04/13/11	L. P.	Updated Supply Current specifications.
N	06/03/11	D.C.	Updated package drawing and dimensions for 8MSOP.
P	06/05/12	D.C.	1. Updated top-side marking for DVG package from 'YWW$' to 'YYWW$'
Q	09/20/12	J. Chao	1. Moved all from Fab4 to TSMC. QA requested change in the marking of only the 16-pin SOIC device with internal crystal to add "A" due to the fact that TSMC uses a different crystal than Fab4. Notification of a change in orderables was initiated with PCN A1208-06. 2. Updated 16-pin SOIC marking diagram and ordering information to include "A".
R	12/10/12	J. Chao	Updated orderable parts - added “G” to 16-pin SOIC parts with SRI/SRI8. New part numbers for 16-pin SOIC will read as SRGI and SRGI8.
S	07/01/13	J. Chao	Updated Typ. and Max. values for Vbackup parameters in DC char table per latest TSMC data.
S	03/10/14	J. Chao	Updated tVCCF from 300 µs to 3 ms. Added associated note.

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