

Document Title

128K x8 bit Low Power CMOS Static RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial draft for commercial product - Commercial Product only	October 28, 1992	Preliminary
0.1	- Initial draft for Extended/Industrial Product - Datasheet for Extended/Industrial Product	September 1, 1993	Preliminary
1.0	Finalized - Commercial product finalized at 1993 - Extended and industrial product finalized at 1994	September 1, 1993 September 24, 1994	Final
2.0	Revised - Change datasheet format : one datasheet for commercial, extended industrial product	April 12, 1996	Final
3.0	Revised - Change datasheet format - Erase 100ns part from extended and industrial product - Erase Low power part from TSOP package	January 20, 1998	Final

The attached datasheets are provided by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications and products. SAMSUNG Electronics will answer to your questions about device. If you have any questions, please contact the SAMSUNG branch offices.



Revision 3.0
January 1998

128K x8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : Poly Load
- Organization : 128Kx8
- Power Supply Voltage : 4.5~5.5V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 32-DIP-600, 32-SOP-525
32-TSOP1-0820F/R

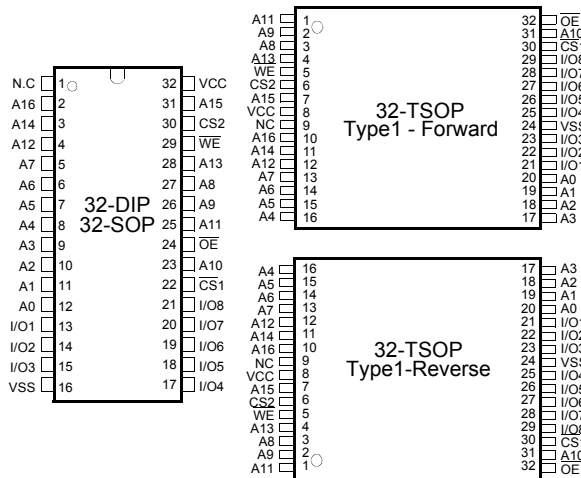
GENERAL DESCRIPTION

The KM681000B families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

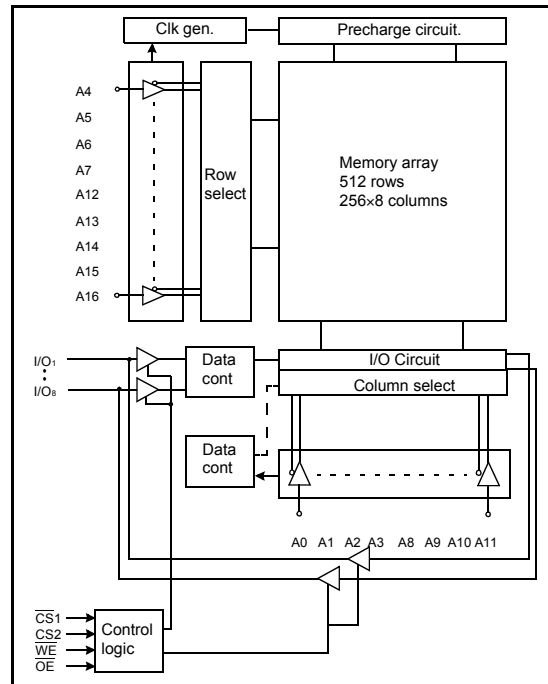
Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I _{sb1} , Max)	Operating (I _{cc2} , Max)	
KM681000BL KM681000BL-L	Commercial(0~70°C)	4.5 to 5.5V	55/70	100µA 20µA	70mA	32-DIP,32-SOP 32-TSOP1 R/F
KM681000BLE KM681000BLE-L	Extended(-25~85°C)		70	100µA 50µA		32-SOP 32-TSOP1 R/F
KM681000BLI KM681000BLI-L	Industrial(-40~85°C)		70	100µA 50µA		32-SOP 32-TSOP1 R/F

PIN DESCRIPTION



Name	Function
$\overline{CS1}, \overline{CS2}$	Chip Select Inputs
\overline{OE}	Output Enable Input
\overline{WE}	Write Enable Input
A0~A16	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temperature Products (0~70°C)		Extended Temperature Products (-25~85°C)		Industrial Temperature Products (-40~85°C)	
Part Name	Function	Part Name	Function	Part Name	Function
KM681000BLP-5	32-DIP,55ns,L-pwr	KM681000BLGE-7	32-SOP,70ns,L-pwr	KM681000BLGI-7L	32-SOP,70ns,LL-pwr
KM681000BLP-5L	32-DIP,55ns,LL-pwr	KM681000BLGE-7L	32-SOP,70ns,LL-pwr	KM681000BLTI-7L	32-TSOP F,70ns,LL-pwr
KM681000BLP-7	32-DIP,70ns,L-pwr	KM681000BLTE-7L	32-TSOP F,70ns,LL-pwr	KM681000BLRI-7L	32-TSOP R,70ns,LL-pwr
KM681000BLP-7L	32-DIP,70ns,LL-pwr	KM681000BLRE-7L	32-TSOP R,70ns,LL-pwr		
KM681000BLG-5	32-SOP,55ns,L-pwr				
KM681000BLG-5L	32-SOP,55ns,LL-pwr				
KM681000BLG-7	32-SOP,70ns,L-pwr				
KM681000BLG-7L	32-SOP,70ns,LL-pwr				
KM681000BLT-5L	32-TSOP F,55ns,LL-pwr				
KM681000BLT-7L	32-TSOP F,70ns,LL-pwr				
KM681000BLR-5L	32-TSOP R,55ns,LL-pwr				
KM681000BLR-7L	32-TSOP R,70ns,LL-pwr				

Note : LL means Low Low standby current.

FUNCTIONAL DESCRIPTION

\overline{CS}_1	CS_2	\overline{OE}	\overline{WE}	I/O Pin	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X ¹⁾	L	Din	Write	Active

1. X means don't care.(Must be low or high state.)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} ,V _{OUT}	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to 7.0	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	KM681000BL
		-25 to 85	°C	KM681000BLE
		-40 to 85	°C	KM681000BLI
Soldering temperature and time	T _{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.5 ²⁾	V
Input low voltage	V _{IL}	-0.5 ³⁾	-	0.8	V

Note

- Commercial Product : T_A=0 to 70°C, unless otherwise specified
 Extended Product : T_A=-25 to 85°C, unless otherwise specified
 Industrial Product : T_A=-40 to 85°C, unless otherwise specified
- Overshoot : V_{CC}+3.0V in case of pulse width≤30ns
- Undershoot : -3.0V in case of pulse width≤30ns
- Overshoot and undershoot are sampled, not 100% tested

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	6	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	8	pF

- Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

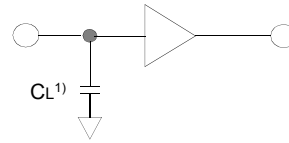
Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Operating power supply	I _{CC}	$\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , I _{IO} =0mA, V _{IN} =V _{IL} or V _{IH}	-	7	15 ¹⁾	mA	
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA, $\overline{CS}_1\leq 0.2V$, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	10 ²⁾	mA	
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH}	-	-	70	mA	
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	V	
Standby Current(TTL)	I _{SB}	$\overline{CS}_1=V_{IH}$, CS ₂ =V _{IL} , Other input=V _{IL} or V _{IH}	-	-	3	mA	
Standby Current(CMOS)	I _{SB1}	$\overline{CS}_1\geq V_{CC}-0.2V$, CS ₂ ≥V _{CC} -0.2V or CS ₂ ≤0.2V Other input=0~V _{CC}	KM681000BL	-	-	100	μA
			KM681000BL-L	-	-	20	μA
		Other input=0~V _{CC}	KM681000BLE	-	-	100	μA
			KM681000BLE-L	-	-	50	μA
Other input=0~V _{CC}	KM681000BLI	-	-	100	μA		
	KM681000BLI-L	-	-	50	μA		

- 20mA for Extended and Industrial Products
- 15mA for Extended and Industrial Products

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.8 to 2.4V
 Input rising and falling time : 5ns
 Input and output reference voltage : 1.5V
 Output load (See right) : $CL=100pF+1TTL$



1. Including scope and jig capacitance

AC CHARACTERISTICS (V_{CC}=4.5~5.5V, KM681000B Family : T_A=0 to 70°C, KM681000BE Family : T_A=-25 to 85°C, KM681000BI Family : T_A=-40 to 85°C)

Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	55	-	70	-	ns
	Address access time	t _{AA}	-	55	-	70	ns
	Chip select to output	t _{CO1,tCO2}	-	55	-	70	ns
	Output enable to valid output	t _{OE}	-	25	-	35	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	20	0	25	ns
	Output disable to high-Z output	t _{OHZ}	0	20	0	25	ns
	Output hold from address change	t _{OH}	10	-	10	-	ns
Write	Write cycle time	t _{WC}	55	-	70	-	ns
	Chip select to end of write	t _{CW}	45	-	60	-	ns
	Address set-up time	t _{AS}	0	-	0	-	ns
	Address valid to end of write	t _{AW}	45	-	60	-	ns
	Write pulse width	t _{WP}	40	-	50	-	ns
	Write recovery time	t _{WR}	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	20	0	25	ns
	Data to write time overlap	t _{DW}	25	-	30	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	ns

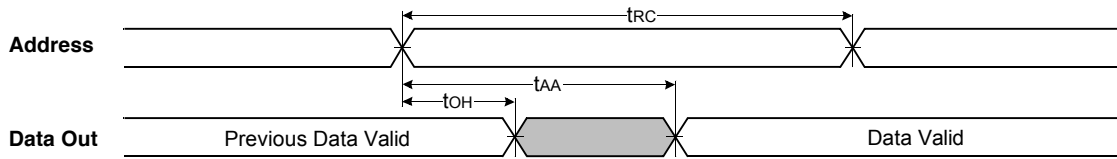
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit	
V _{CC} for data retention	V _D R	$\overline{CS}_1 \geq V_{CC}-0.2V$	2.0	-	5.5	V	
Data retention current	I _D R	V _{CC} =3.0V $\overline{CS}_1 \geq V_{CC}-0.2V$, CS ₂ ≥ V _{CC} -0.2V or CS ₂ ≤ 0.2V Other Input+0~V _{CC}	KM681000BL	-	1	50	μA
			KM681000BL-L	-	0.5	10	
			KM681000BLE	-	-	50	
			KM681000BLE-L	-	-	25	
Data retention set-up time	t _R D _R	See data retention waveform	0	-	-	ms	
			5	-	-		
Recovery time	t _R D _R						

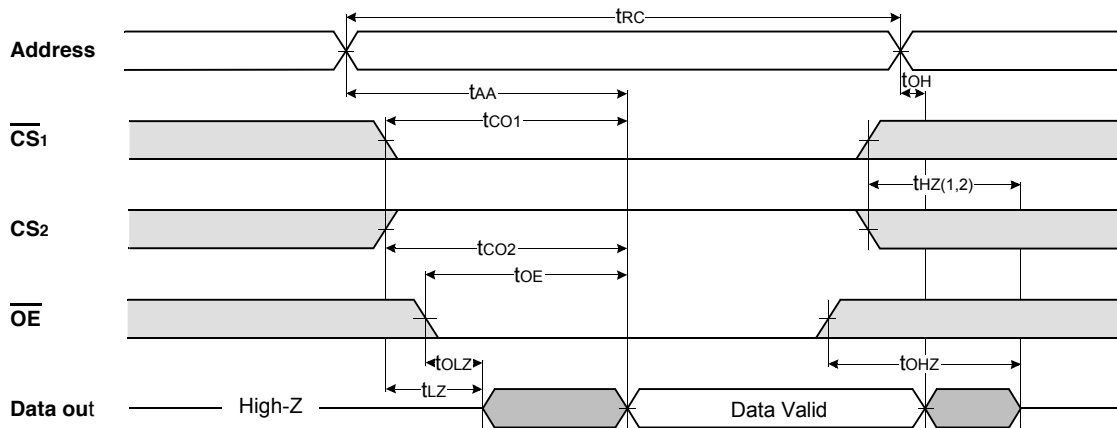
1. $\overline{CS}_1 \geq V_{CC}-0.2V, CS_2 \geq V_{CC}-0.2V$ (\overline{CS}_1 controlled) or $CS_2 \leq 0.2V$ (CS_2 controlled)

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)



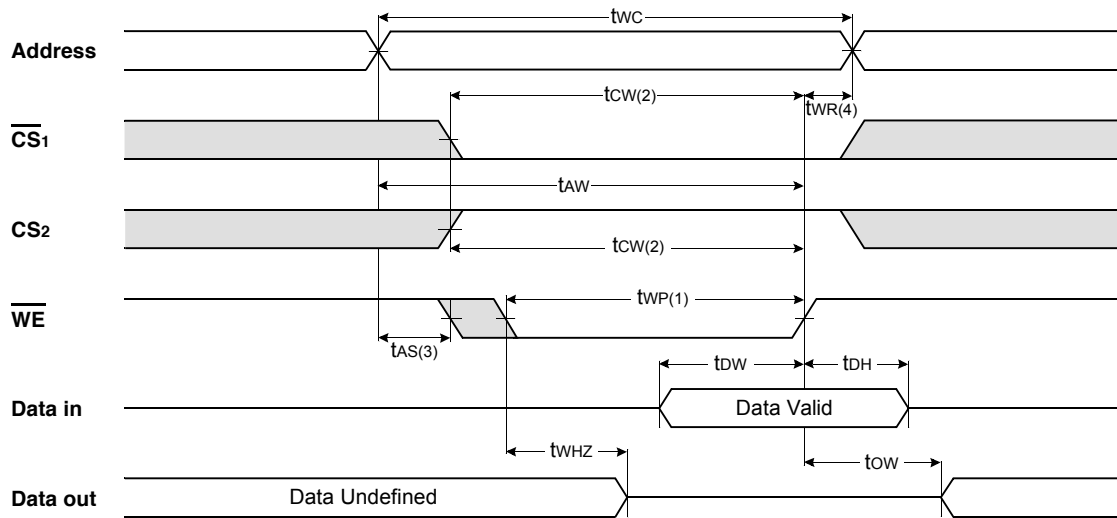
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



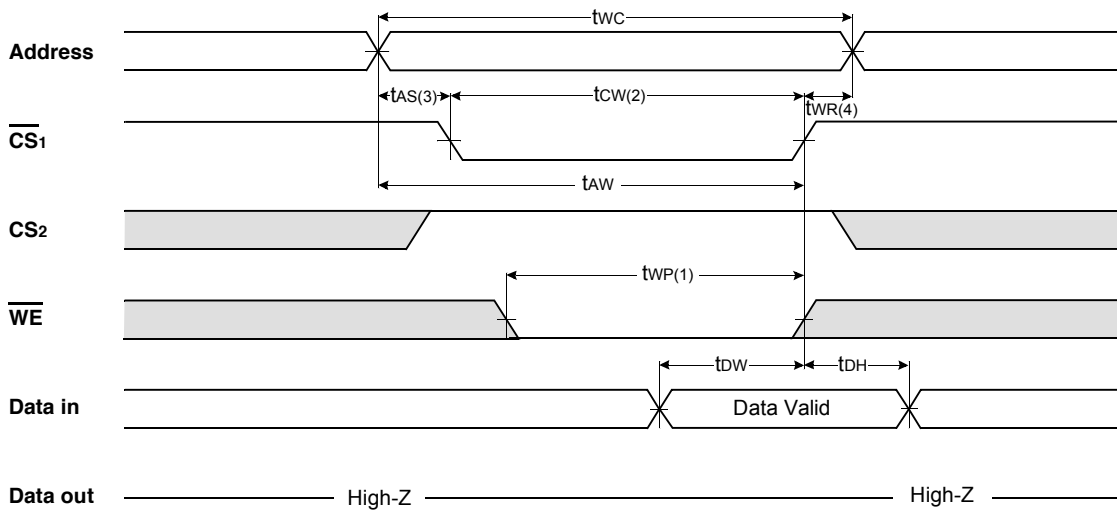
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

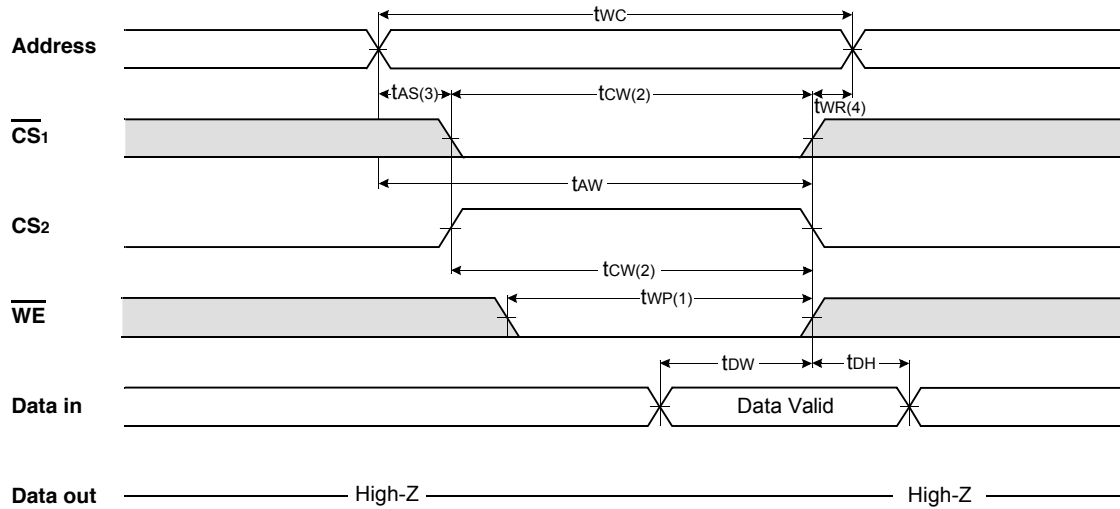
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)

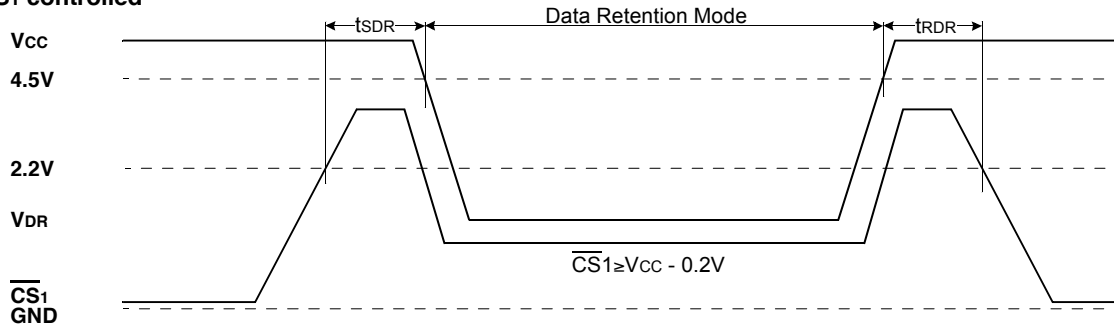


NOTES (WRITE CYCLE)

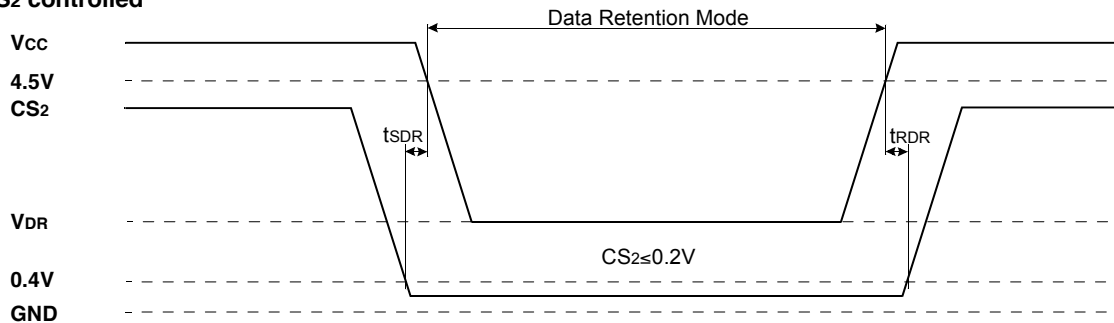
1. A write occurs during the overlap of a low $\overline{CS1}$, a high $CS2$ and a low \overline{WE} . A write begins at the latest transition among $\overline{CS1}$ goes low, $CS2$ going high and \overline{WE} going low : A write end at the earliest transition among $\overline{CS1}$ going high, $CS2$ going low and \overline{WE} going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}$ going low or $CS2$ going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. $t_{WR(1)}$ applied in case a write ends as $\overline{CS1}$ or \overline{WE} going high $t_{WR(2)}$ applied in case a write ends as $CS2$ going to low.

DATA RETENTION WAVE FORM

$\overline{CS1}$ controlled



CS2 controlled



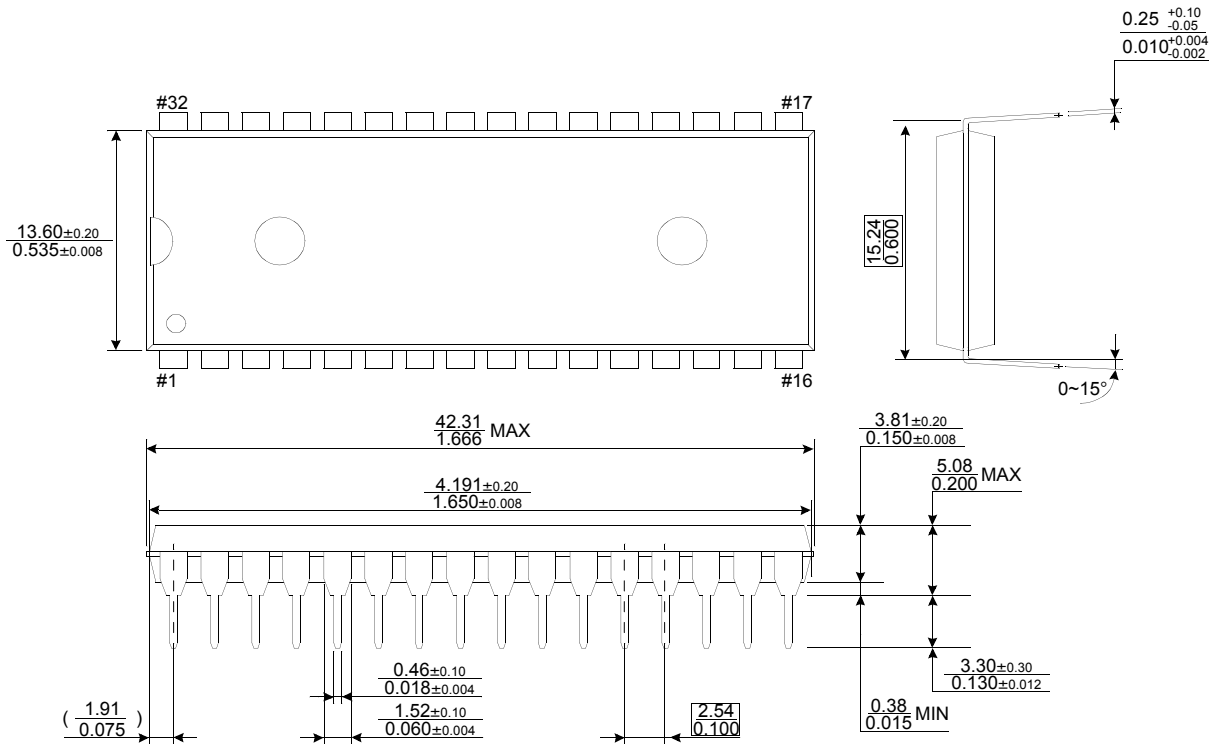
KM681000B Family

CMOS SRAM

PACKAGE DIMENSIONS

Units : millimeter(inch)

32 DUAL INLINE PACKAGE (600mil)



32 PLASTIC SMALL OUTLINE PACKAGE (525mil)

